

A High Efficient Cross-Coupled Active Rectifier by Using High Speed Switching Comparators for Wireless Power Receiver

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ABSTRACT This paper introduces a highly efficient cross-coupled active rectifier with fast switching comparators for wireless power transfer (WPT) system. Wireless power transfer technology is increasingly being utilized in various applications. In our proposed design an active diode switches are introduced at lower side of power MOSFET to minimize the switching delay in power transistors and also reduces reverse leakage current to boost power conversion efficiency. The active diode is constructed from high-speed comparators and CMOS power switches. A cross-coupled technique is applied to the high side PMOS power transistors, in order to minimizing power consumption and optimizing current management. This enhancement not only improves the power efficiency of the cross-coupled active rectifier but also prolongs battery life and boosts the overall Efficiency. The cross-coupled architecture of the proposed rectifier enables high-speed switching, which is necessary for its design. This allows for fast response times and efficient signal processing. The presented cross-coupled active rectifier is designed using 0.18 μm CMOS technology. It delivers 2.77 W of output power using a 1 μF capacitor with a 0.3A load current, and it achieves a power efficiency of 92.4%.

INDEX TERMS High efficiency, WPT, unbalanced size comparators, switching, rectifier, cross-coupled.

I. INTRODUCTION

WIRELESS power transfer (WPT) techniques are extensively applied across various field such as consumer electronics, industry, transportation and for medical devices [1], [2], [3]. Wireless Power Transfer (WPT) has evolved into a crucial technology, particularly in the development of wireless charging systems for a diverse range of devices, including those connected to the Internet of Things (IoT). In recent years, the IoT has significantly influenced portable electronics, leading to higher power demands to maintain advanced functionalities. Despite this,

advancements in battery life and charging technologies have lagged behind the needs of the IoT.

It is essential for good power management, that considers the power source, battery life and device size as well. However, the efficiency of WPT systems can be compromised by multistage power processing. Recent research has focused on exploring various topologies to enhance the efficiency of these systems [4]. The primary objective in WPT research is to achieve high efficiency [5], [6], [7], [8]. A goal that has motivated ongoing studies aimed at developing more effective power management strategies to

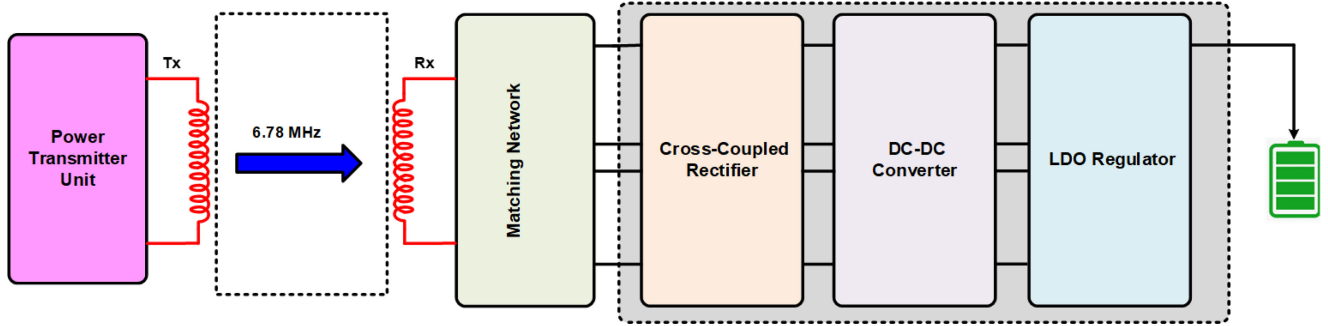


FIGURE 1. Block diagram of a wireless power transfer system.

meet system demands and address specific power needs [5], [9], [10]. Such improvements are essential for extending battery life and reducing device size, thereby increasing user flexibility [11]. In practical applications, different types of rectifier converters are employed based on specific user requirements, but the main goal is to optimize for high efficiency, compact size, and minimal power consumption. In typical WPT systems, as illustrated in Fig. 1, the power conversion process includes a front-end rectifier to convert AC to DC, followed by a buck or boost DC-DC converter to regulate the dc voltage. The overall efficiency of a WPT system depends on the rectifier ability to efficiently extract and convert power, as well as the performance of the DC-DC converter. Therefore, employing a high-performance rectifier with superior power extraction and conversion capabilities is crucial for enhancing the efficiency of WPT systems.

In this paper, we propose an active rectifier to enhance the power conversion efficiency significantly. The design includes a high-speed comparator-based cross coupled active rectifier, which is among the most effective solutions for addressing the forward voltage drop commonly observed in traditional rectifiers. Active synchronous rectifiers that utilize comparator-controlled rectifying switches are currently viewed as highly promising in this respect. However, the comparators based active rectifiers that can experience significant leakage issues during high-frequency operations. This is primarily due to the delays in turning on and off the main power transistors within the rectifier. To address this challenge, we introduce a high-speed comparator-based cross-coupled active rectifier. This new approach aims to reduce leakage problems by minimizing the turn-on and turn-off delays, thereby improving overall efficiency.

II. STATE OF THE ART RECTIFIER DESIGNS

Fig. 2 illustrates the most commonly utilized rectifier configurations. Among these, the simplest and most robust are the diode and transistor-configured diode rectifiers shown in Fig. 2(a) and 2(b) [12]. Fig. 2(e) depicts a conventional full-wave rectifier, consisting of either four diodes or MOS transistors configured as diodes. This type of rectifier begins functioning when the input voltage exceeds two threshold voltages, namely the forward voltage drops (VD) of the

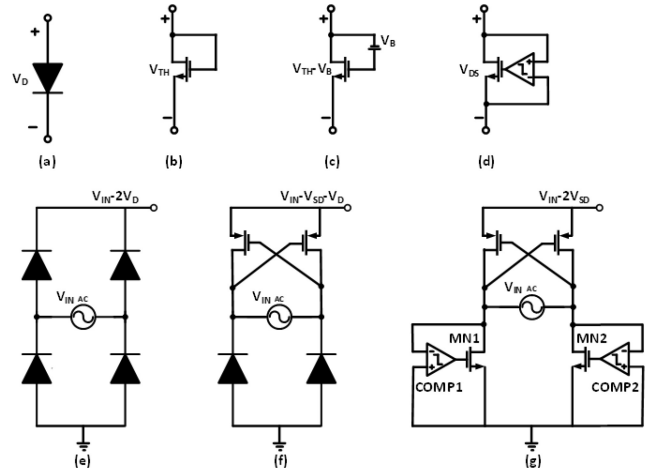


FIGURE 2. (a) Diode. (b) Diode-connected. (c) VTH-cancellation. (d) Comparator-controlled. (e) Diode-based. (f) Cross-coupled. (g) Active cross-coupled rectifier.

diodes. Given a typical NMOS transistor threshold voltage of 0.5 V, this can significantly lower the output voltage from the rectifier and reduce overall power efficiency. One method to decrease the VD involves superimposing a bias voltage VB onto the gate of the MOSFET, effectively neutralizing the drop caused by the threshold voltage VTH, as shown in Fig. 2(c) [12]. However, this approach needs an extra voltage generator circuit, which makes the rectifier design more complicated.

Alternatively, a comparator-controlled rectifier can be used to minimize the voltage drop issue [13], as depicted in Fig. 2(d). In this setup, a NMOS transistor functions as a switch to regulate conduction in the forward path. If the input voltage exceeds the output voltage, the comparator output turns positive and activates the switch, allowing charge to flow to the output load. On the other hand, the comparator output becomes negative if the input voltage is lower than the output voltage, deactivating the switch and disconnecting the forward conduction path. This approach significantly reduces the diode voltage drop, although designing an ultra-low power comparator remains a challenge. If the power consumed by the comparator is too high, it could cancel out the benefits of a lower diode voltage drop.

Moreover, since the input from the transducer is AC, cross-coupling complementary inputs can drive and enhance the gates of the rectifying transistors as shown in Fig. 2(f) [14], but still there is voltage drop across the diode which reduce the efficiency. Fig. 2(g) [15], introduces a cross-coupled rectifier paired with an unbalanced comparator-controlled rectifier for improved PCE.

Section III, of this paper proposes an active rectifier with an unbalanced size comparator, which improve power conversion efficiency and forward voltage drop.

III. ACTIVE RECTIFIER WITH UNBALANCE SIZE COMPARATOR

The structure design for the rectifier with an unbalanced size comparator is shown in Fig. 2(g). Our design uses two active diodes instead of traditional passive diodes to minimize significant voltage losses and enhance the rectifier efficiency. The configuration includes NMOS and PMOS input transistors in the unbalanced size comparators, which are more effective at reducing conduction losses than passive diodes and standard comparators. These active components typically exhibit lower forward voltage drops, contributing to decreased power losses by limiting reverse leakage current and boosting overall efficiency. Additionally, they are capable of switching on and off more rapidly than passive diodes and provide precise control over the rectification process, thus allowing for improved regulation of the output voltage and enhanced performance.

The unbalanced comparators activate and deactivate the MOS switches, M_{N1} and M_{N2} . The switch M_{N1} is turned on when V_{AC} is greater than comparator $COMP_1$. Similarly, when V_{AC} is lower than comparator $COMP_2$ will turn on the M_{N2} . The size of the comparators and switching transistors plays a crucial role in optimizing the rectifier efficiency. Increasing the size of the transistors reduces the turn-on resistance, which in turn lowers conduction losses. However, the parasitic capacitance associated with larger transistors can increase switching losses. The comparator performance has a big impact on the rectifier efficiency as well. Fig. 3(a) and 3(b) illustrate the proposed unbalance comparators. To reduce drain leakage in the proposed unbalance comparator, we selected minimum-sized transistors in non-critical paths and used higher threshold voltage devices where speed was not the primary concern. Additionally, we optimized the transistor aspect ratios (W/L) to ensure that transistors operate efficiently in the subthreshold or near-threshold region when appropriate, helping to limit leakage and improve efficiency. In engineering design, offset is an important measurement used to evaluate how well a comparator performs. Although there is intentional mismatch in input transistor sizing for offset calibration, we carefully optimized this mismatch to remain within a range that does not significantly worsen kickback-induced charge injection. Pre-amplifier stage is used to isolate the core comparator from the signal source and to reduce kickback coupling. By using a comparator with an active diode facilitates the fast switching of transistors on

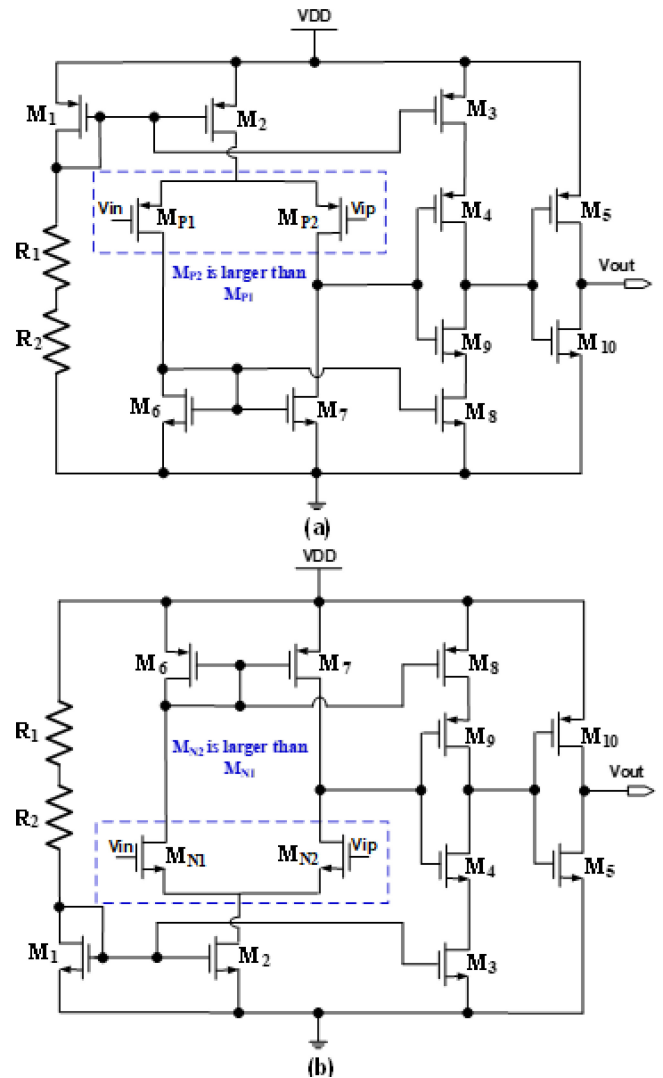


FIGURE 3. Unbalance-Size Comparator (a) PMOS input transistor (b) NMOS input transistor.

and off, thereby reducing voltage drop. However, as indicated by the simulation results of the unbalanced comparator in Fig. 4, delay in the comparator can not prevent the active diodes from blocking reverse currents effectively, leading to conversion losses. To mitigate this issue and enhance the PCE of our rectifier, we have designed a new high-speed comparator shown in Fig. 7, utilizing these unbalanced size comparators in our proposed active rectifier setup.

IV. PROPOSED ACTIVE RECTIFIER

Fig. 5 shows the schematic of the proposed active rectifier utilizing a cross-coupled topology. In this design, we implemented an off-chip matching network to ensure optimal power transfer and minimize reflection loss at the operating frequency of 6.78 MHz. The performance of matching network validated through S11 is -80dB shown in Fig. 6. The open loop delay (OPLD) circuit technique is used in proposed high speed comparator to trade-off between power and speed. The lower two NMOS transistors are substituted

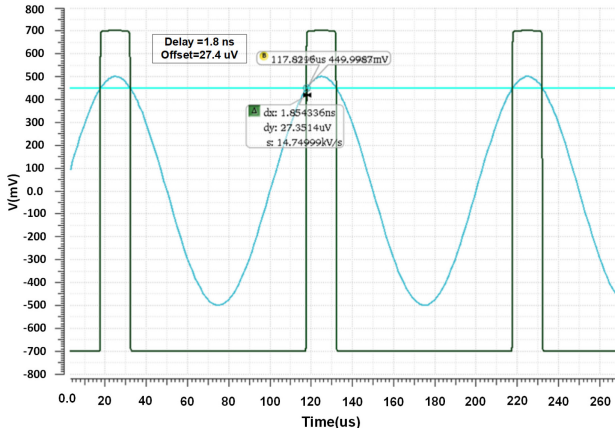


FIGURE 4. Simulation Result of Unbalance Comparator.

with a high-speed comparator-based active switches, which help to minimize the on and off switching issues that typically lead to leakage current in rectifier and reduce the PCE. This cross-coupled active rectifier transforms V_{AC} voltages (V_{AC1} and V_{AC2}) into a dc output (V_{RECT}). In this design, P-channel metal-oxide semiconductor (PMOS) cross-coupled structures are used to minimize switching losses in high-side core implementations [9], [16], [17]. Even though, PMOS has less mobility than NMOS, it is still advantageous to enlarge PMOS transistors in order to reduce the voltage drop between the drain-source (VDS) [18], [19]. Conversely, to maintain a compact core size while still achieving a low VDS voltage drop, NMOS transistors are also preferred for the high-side core [20]. Three states describe the operation of the proposed rectifier: first, all four power transistors (M_{N1} , M_{N2} , M_{P1} , M_{P2}) are off when the input voltage is very low but greater than zero. As the differential input voltage increases and reaches the threshold voltage of transistors M_{P1} or M_{P2} , the corresponding PMOS switch turns on, effectively connecting the respective input terminal (V_{AC1} or V_{AC2}) to V_{RECT} . Further increases in the input voltage lead to a decrease in the voltage difference across the opposite terminal, reducing the corresponding differential voltage. When the negative input to the comparator drops below ground, the comparator output turns positive, activating the switch and allowing charge to flow to the output load. This comparator-controlled approach significantly reduces the voltage drop typically associated with diodes. However, during high-frequency operations, delays in the turning on and off of the main power transistors can lead to leakage current, adversely affecting the PCE of the rectifier. To address this, a new high speed comparator design shown in Fig. 7, with unbalanced size comparators used in proposed active rectifier.

A. PROPOSED HIGH SPEED COMPARATOR

The Proposed high-speed comparator is used open loop delay (OPLD) circuit, to minimize the reverse leakage currents produce by the turning on and off of power MOSFETs,

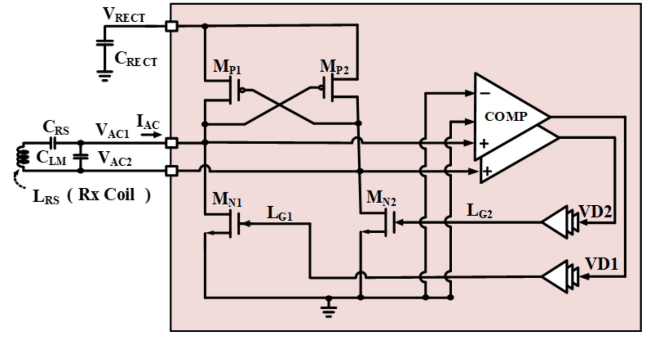


FIGURE 5. Block diagram of Active Rectifier.

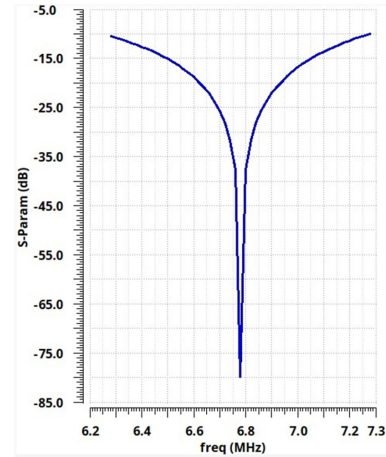


FIGURE 6. Simulation results of matching network.

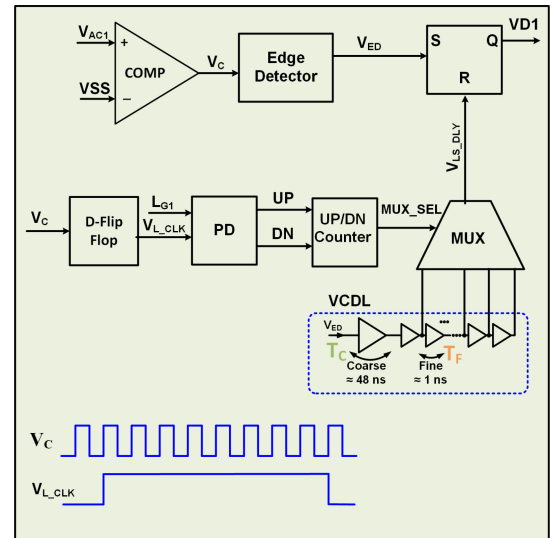


FIGURE 7. Block Diagram of high speed comparator.

and enhance PCE [21], [22], [23]. In Fig. 7, an input AC voltage (V_{AC}) is supplied externally to an unbalanced size comparator. These comparators produce delays when the power MOSFET switches turn ON/OFF within the core block of the rectifier, which results in the generation of reverse leakage currents and minimize the PCE. To reduce

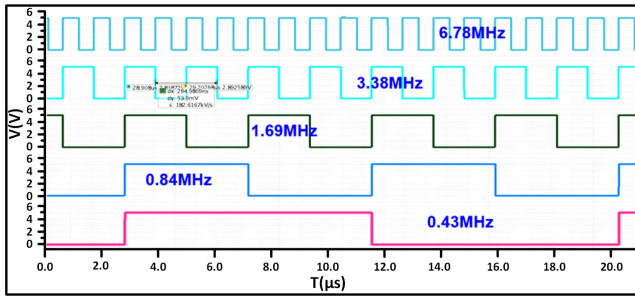


FIGURE 8. Simulation result Of D-flip flop.

this, delay the design includes, an edge detector (V_{ED}), a phase detector (PD), a D-flip flop (D- FF) equipped with a divided-by-8, coarse and fine delay cells, a multiplexer (MUX), and an SR latch make-up the high-speed comparator. The role of this comparator is to synchronize the driver output falling edge L_{G1} with the zero-crossing point of the AC signal, V_{AC1} . This synchronization allows M_{N1} to turn off when V_{AC1} transitions from positive to negative, effectively minimizing the reverse leakage current. The falling edges of V_{L-CLK} and L_{G1} , which represent the voltage signal of V_{AC1} and the final gate control signal of M_{N1} respectively, are compared using a PD. The falling edge of the control signal V_C is generated as V_{LS-DLY} because the signal is delayed by the coarse and fine delay cells which initially came from V_{ED} . This intricate design helps maintain the efficiency of the rectifier by precisely controlling the timing of power switches to reduce leakage currents significantly.

In the high-speed comparator, a coarse delay line is implemented to push the loop toward the lock state, while a fine delay line performs minor adjustments to the output phase. The input to the coarse delay line is derived from the output of the edge detector. Ten delayed signals are sent into the multiplexer (MUX) after passing through coarse and fine delay cells. The PD can choose a signal among the 10 delayed signals to use by adjusting the MUX [3:0] parameters with this arrangement, V_C and L_{G1} falling edges coincide. A 57-ns delay is provided by the coarse delay, while a 1-ns adjustment is provided by the fine delay. After a comparison in which $VD1$ and $VD2$ functions are reversed, it takes some time for the rectifier internal signals to stabilize.

As shown in Fig. 8, frequency of V_C is split by 8, and the rectifier settling time is accommodated by using this divided frequency as the PD clock. The PD compares two voltage signals, D_{L-CLK} and L_{G1} , and generates two outputs, UP and DN, that represent the phase difference between the two signals. Even though L_{G1} contains eight falling edges, the PD only looks at phase differences and chooses the nearest edge for comparison. The DN should ideally be low and the UP signal active, and vice versa. The counter stops the counting when the falling edges of V_{L-CLK} and L_{G1} synchronize. The PD adds the value of MUX [3:0] if the V_{L-CLK} falling edge lags behind L_{G1} , this increases the

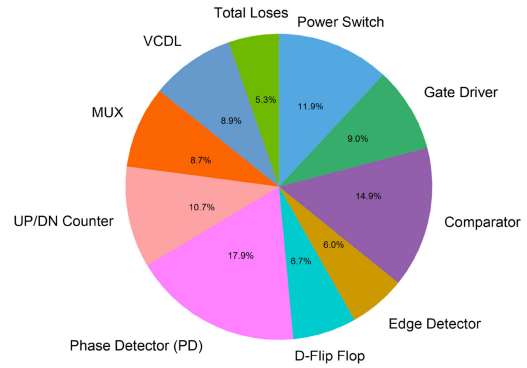


FIGURE 9. Power consumption of the Proposed Rectifier.

delay. On the other hand, the PD reduces the delay if the V_{L-CLK} falling edge occurs before the L_{G1} by subtracting the value of MUX [3:0]. V_{LS-DLY} functions as a reset signal, while V_{ED} is employed as a set signal used as input of SR latch and this generates $VD1$, which is subsequently applied to the gate driver input. Until the falling edges of V_{L-CLK} and L_{G1} are synchronized, the PD comparison procedure is repeated continuously. This process reduces reverse leakage current and improves the circuit PCE. The pie diagram of the power consumption of each block of proposed high speed comparator including power switches and gate drivers is shown in Fig. 9. Fig. 10, illustrates the timing diagram of the proposed high-speed comparator-based rectifier, which is designed to minimize reverse leakage current by ensuring that the power MOSFET switches turn on and off precisely at the zero-crossing points of the input AC voltage (V_{AC1}). The input signal V_{AC1} is sensed by a high-speed comparator (as shown in Fig. 7), which detects the zero-crossing instant. An edge detector processes the comparator output and generates a narrow pulse (V_{ED}) at each zero-crossing transition. In the timing diagram, $V_{LG1-DLY}$ represents the delay signal for the power MOSFET M_{N1} , before introduction of the high-speed comparator, M_{N1} would switch off after the zero-crossing point of V_{AC1} , resulting in reverse leakage current. In the enhanced design, the V_{LS-DLY} signal generated at the output of the MUX, is used as the reset signal to an SR latch, while V_{ED} serves as the set signal. The output of this latch, L_{G1} , directly drives the gate of M_{N1} without any delay. This configuration ensures that M_{N1} turns off exactly at the zero-crossing point of V_{AC1} , thereby minimizing reverse leakage current and significantly improving PCE. Table 1 shows the power analysis of rectifier. Fig. 11 shows a simulation result of the proposed cross-coupled active rectifier.

V. MEASUREMENT RESULTS

The measuring configuration for the Wireless Power Transfer (WPT) system is shown in Fig. 12. Magnetic fields help this system to transfer the energy between primary (Tx) and secondary (Rx) coil. A high-frequency alternating current flows through the Tx coil, generating an electromagnetic field. The TRx matching efficiency measured system is

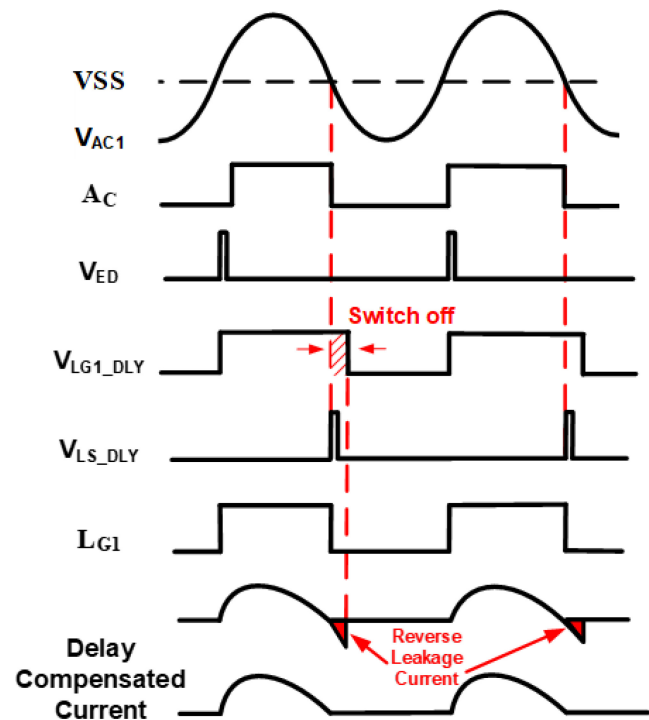


FIGURE 10. Timing diagram of high speed comparator.

TABLE 1. Power analysis of rectifier.

Parameters	Rectifier with unbalanced comparators	Proposed Rectifier
Conduction losses	5.4 %	4.7 %
Switching losses	4 %	0.59 %
Gate drive losses	3.2 %	1.06 %
Internal circuit losses	3.8 %	1.25 %
Total losses	16.4 %	5.3 %
Input power	3 W	3 W
Output power	2.508 W	2.77 W
Efficiency	83.6 %	92.4 %

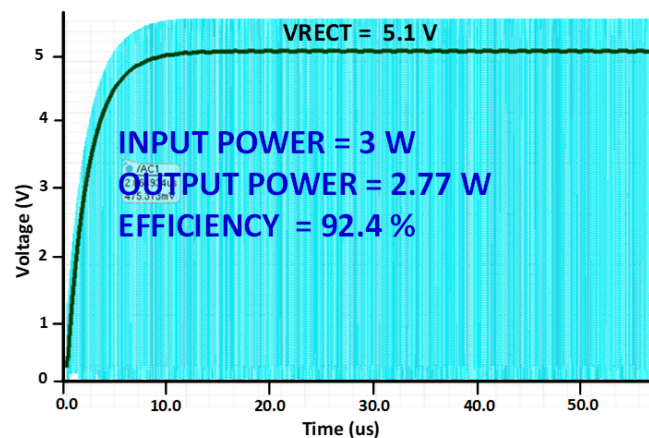


FIGURE 11. Simulation results of the Proposed Rectifier.

shown in Fig. 13, it approximately 94% average transfer efficiency. Optimal power transfer occurs when both coils resonate at the same frequency. The Rx coil is positioned beneath the Tx coil, and the measurement environment

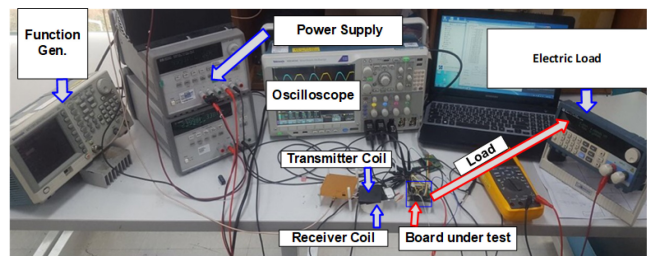


FIGURE 12. Measurement setup of WPT system.

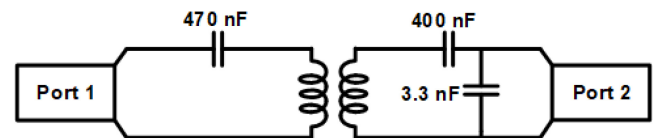
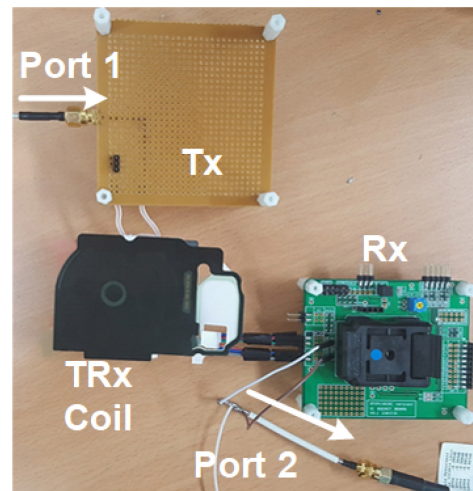


FIGURE 13. TRx Matching Efficiency Measurement.

includes components such as a oscilloscope, a power supply, an electronic load, a function generator, and the test board. Fig. 14 shows a microphotograph of the proposed chip, the active die area of the cross-coupled active rectifier is measured 820 μm by 940 μm . Fig. 15 shows the measurement results for the cross-coupled active rectifier equipped with a high-speed comparator. The measured output voltage (V_{RECT}) of the active rectifier is 5 V with achieving an efficiency of 92.4%. Fig. 16 compares the efficiencies of the cross-coupled active rectifier using the proposed high-speed comparator with those of an unbalanced comparator across different load currents. The active rectifier achieves its maximum efficiency of 92.4% at a load current of 300 mA with the proposed high-speed comparator. In our proposed high speed comparator input-referred offset voltage is measured to be 7.36 μV . The comparator was optimized for fast response and minimal offset to ensure accurate switching at the zero-crossing point. The effective hysteresis is negligible, limited only by intrinsic regenerative delay and device-level mismatches, and is estimated to be less than 1 mV.

TABLE 2. Performance comparison with prior works.

Parameters	[6]	[7]	[8]	[15]	[17]	[19]	This Work
Technology (nm)	180	180	350	350	350	180	180
Output Voltage (V)	8.62	8.66@A4WP/6.85@WPC	5	2.28	3.52	5	5
Output Power (W)	6	6.87	6	—	24.8m	0.82	2.77
Rectifier load value (A)	0.8	0.6	—	0.2	—	0.1	0.3
Applied frequency (MHz)	6.78	6.78/0.085-0.5	6.78	1.5	13.56	6.78	6.78
Mode	Single	Triple	Single	Single	Single	Single	Single
Efficiency (%)	91.5	91.7	86	87	90.1	82.14	92.4

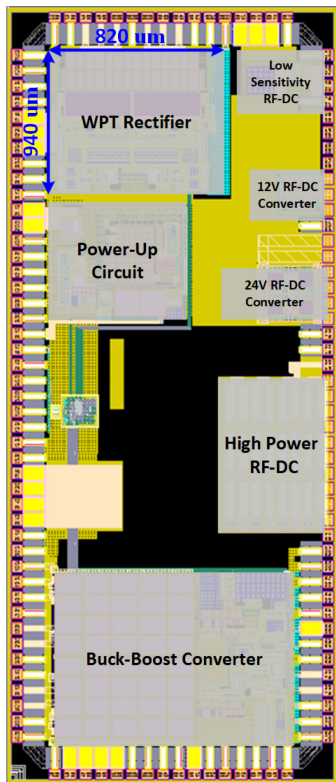


FIGURE 14. Microphotograph of the proposed chip.

Table 2 shows, a comparison of this research work with recent studies as in [6], [7], [8], [15], [17] and [19]. This article demonstrates that the PCE of the cross-coupled active rectifier with proposed high-speed comparators, exceeds that of previous work.

VI. CONCLUSION

This article presents the design of a cross-coupled active rectifier for wireless power transfer (WPT) applications. The design includes a high-efficiency cross-coupled configuration that utilizes a high-speed comparator. It addresses power transistor switching delays by employing an active diode structure, which reduces reverse leakage current and enhances PCE. The rectifier has been implemented using a 0.18- μm bipolar-CMOS DMOS process. Its cross-coupled architecture allows for rapid response times, facilitating fast signal processing. With a 1 μF output capacitor and a

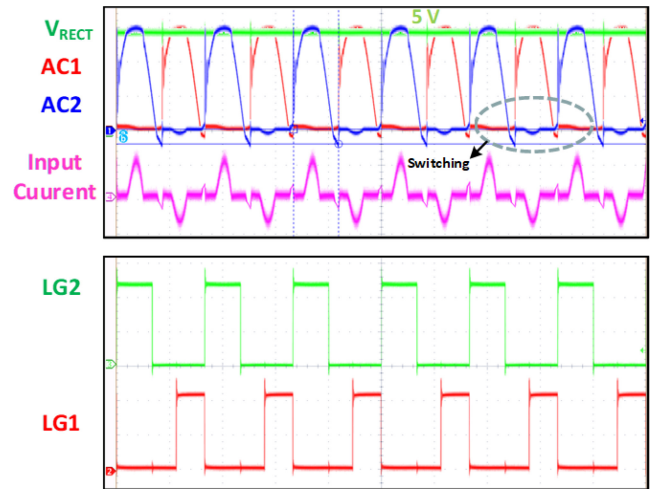


FIGURE 15. Measurement Result of Rectifier.

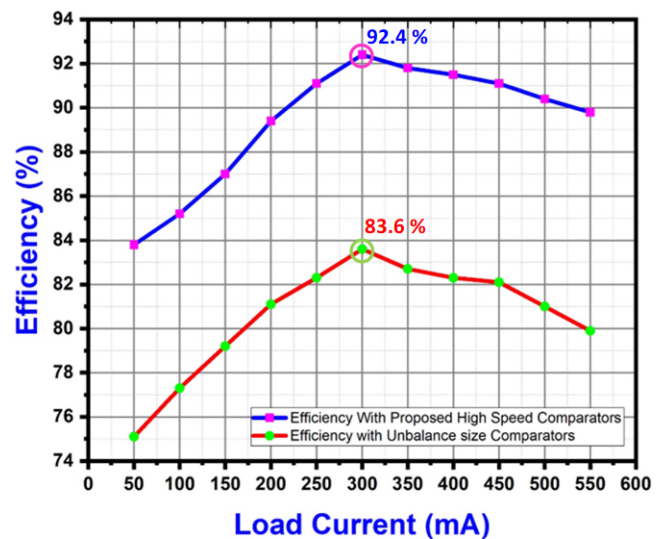


FIGURE 16. Measured Efficiency of Rectifier with respect to load current.

0.3A load current, the rectifier generates an output power of 2.77 W while achieving a power efficiency of 92.4%.

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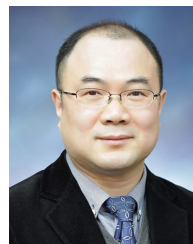
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