



High-performance full-swing a-HfInZnO inverter and advanced integrated logic circuits

Sandeep Kumar Maurya ^{a,b}, Eun Ji Yang ^{a,b}, Sang Yeol Lee ^{a,b,*}

^a Department of Semiconductor and Electronic Engineering, Gachon University, Seongnam-si, 13120, Gyeonggi-do, Republic of Korea

^b Gachon Advanced Institute of Semiconductor Technology (GAIST), Gachon University, Seongnam-si, 13120, Gyeonggi-do, Republic of Korea

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ABSTRACT

We report the fabrication and characterization of high-performance, full-swing inverter and logic circuits based on amorphous hafnium-indium-zinc-oxide (a-HIZO) thin film transistors (TFTs) with varying channel layer thicknesses. Structural and compositional analyses were performed to validate the amorphous nature and chemical uniformity of the HIZO matrix. High-resolution transmission electron microscopy (HRTEM) confirmed the absence of crystallinity. Energy-dispersive X-ray spectroscopy (STEM-EDX) elemental mapping revealed homogeneous distribution of Hf, In, Zn, and O, supporting the multicomponent oxide system. X-ray photoelectron spectroscopy (XPS) analysis was conducted to investigate the elemental composition and oxidation states of Hf, In, Zn, and O. The transmission line method (TLM) was utilized to ensure ohmic contact between the electrodes and the channel layer, and to calculate total resistance, sheet resistance, and contact resistance. The TFTs demonstrated excellent electrical performance, including a maximum field-effect mobility of $13.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on/off current ratio of 10^8 , and stable operation under temperature stress. The a-HIZO-based inverters achieved a maximum voltage gain of 32.38 at a supply voltage of 16 V. In addition, logic circuits, such as NOR and NAND gates, were fabricated, showcasing sharp transfer characteristics. These results highlight the potential of a-HIZO TFTs for advanced electronic applications.

1. Introduction

Thin film transistors (TFTs) are essential technology for advancing next-generation electronics, providing easy fabrication on diverse substrates and being cost-effective. There present several advanced TFT technologies such as amorphous-Si (a-Si:H), organic, low-temperature polycrystalline Si (LTPS), and amorphous oxide semiconductors (AOS). Among these technologies, Si based TFTs are considered cutting-edge technology and are predominantly used in Complementary Metal-Oxide-Semiconductor (CMOS) circuits. However, fabricating LTPS and single crystal Si-based TFT requires temperatures exceeding 450°C . Although, a-Si:H and organic TFTs can be fabricated at relatively lower temperatures than c-Si TFTs, they exhibit poor electrical performance. AOS offer a promising alternative to silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) circuits [1–3]. AOS based TFTs, particularly those using amorphous-In-Zn-O (a-IZO) are recognized for their excellent device performance and ease of fabrication on diverse substrates due to their low processing temperature (below 200°C). These a-IZO TFTs demonstrate a field-effect mobility of $>10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an excellent sub-threshold swing of less than 0.3

V-decade⁻¹, an on-off current ratio exceeding 10^8 , and low operation voltage, among other advantages [4–6]. a-IZO-based TFTs have already been commercialized for use in active-matrix flat-panel displays (AM-FPDs) such as active-matrix liquid crystal displays (AMLCD), high-resolution large-size active-matrix organic light-emitting diode (AMOLED) TV panels.

A CMOS inverter primarily consists of p-channel and n-channel TFTs functioning as pull-up and pull-down devices, respectively [7–11]. However, oxide-TFT-based inverters, such as unipolar n-type metal-oxide-semiconductor (NMOS) inverters, require only n-channel TFTs. Numerous efforts have been made to develop TFT-based inverters and related circuit applications, including logic gates (NAND, NOR gates), ring oscillators (RO), flip-flops, shift registers, and radio-frequency identification (RFID) tags [12–14]. The limited availability of high-performance p-type channel oxide-TFTs has led to the predominance of NMOS inverters, constructed exclusively with n-channel oxide-TFTs, in most oxide-TFT-based applications. These inverters can be categorized into two types: enhancement-mode (E-mode) and depletion-mode (D-mode). Among these, depletion-mode inverters stand out due to their superior performance, which includes low power consumption, sharp

* Corresponding author.

E-mail addresses: sandeep@gachon.ac.kr (S.K. Maurya), ydoymdswl@gachon.ac.kr (E.J. Yang), sylee2020@gachon.ac.kr (S.Y. Lee).

transition characteristics, and a more compact layout [13]. Furthermore, the use of only unipolar TFTs simplifies the fabrication of various logic circuits. Achieving this requires adjusting the threshold voltage through methods such as doping the channel, varying the channel length and width, modifying the channel thickness, and/or altering the electrode configuration [15–18].

In this study, we have fabricated an inverter, as well as NAND and NOR logic circuits, utilizing thin-film transistors (TFTs) with an a-HIZO channel layer. To the best of our knowledge, this is the first reported instance of inverters and logic circuits based on a-HIZO TFTs. The selection of a-HIZO as the channel material was driven by its exceptional electronic properties, including high field-effect mobility and thermal stability, which make it a promising candidate for advanced semiconductor applications [19–22]. To modulate the threshold voltage of the TFTs, we varied the thickness of the channel layer. The a-HIZO TFTs demonstrated excellent electrical properties and high stability under temperature stress. Specifically, the a-HIZO TFTs exhibited a maximum field-effect mobility exceeding $13 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on/off current ratio greater than 10^8 , and an excellent sub-threshold swing (SS) value.

2. Experimental

Bottom gate and top contact a-HIZO TFTs were fabricated using RF magnetron sputtering at room temperature. The devices were configured as shown in Fig. 1. The a-HIZO TFTs were fabricated with different thicknesses via varying deposition time. Deposition was carried out on a 100 nm $\text{SiO}_2/\text{p}^{++}\text{-Si}$ substrate, with SiO_2 serving as the gate insulator. The $\text{SiO}_2/\text{p}^{++}\text{-Si}$ substrates underwent sequential cleaning with acetone, methanol, and DI water for 10 min each in an ultrasonication bath, followed by drying with N_2 gas.

The deposition chamber's base pressure before each deposition was approximately 5×10^{-6} torr. Deposition power, pressure, and Ar flow for all depositions were maintained at a constant 20 W, 16 mT, and 30 sccm, respectively. Devices were fabricated with deposition times of 10 min and 18 min to achieve modulation in the threshold voltage. Fig. 1(b) shows a cross-sectional high-resolution transmission electron microscopy (TEM) image of a control sample, where the a-HIZO channel layer was deposited for 10 min on the SiO_2 gate insulator, followed by an Al_2O_3 capping layer to protect the a-HIZO layer. The a-HIZO layer deposited during the 10 min process has an estimated thickness of approximately 10 nm, indicating a growth rate of 1 nm per minute. Therefore, the channel deposited for 18 min is projected to have a thickness of approximately 18 nm.

Comprehensive structural and compositional characterization was performed using X-ray photoelectron spectroscopy (XPS) over a binding energy range of 0 to 1400 eV to identify the elemental composition and determine the oxidation states of Hf, In, Zn, and O in the HIZO thin film. In addition, X-ray diffraction (XRD), high-resolution transmission electron microscopy (HRTEM), and scanning transmission electron microscopy with energy-dispersive X-ray spectroscopy (STEM-EDX) elemental mapping were employed to evaluate the crystallographic structure and spatial distribution of elements within the film.

After deposition of a-HIZO, the bilayer thin film underwent wet etching process to form channel with width of 250 μm and length of 50 μm . Following channel patterning, films were annealed in air at 150 $^\circ\text{C}$ for 2 h. The source and drain electrodes (S/D) were deposited via e-beam evaporation (10 nm thick Ti) and thermal evaporation (40 nm thick Al) followed by lift-off process.

The electrical characteristics and the stability were carried out in the dark box using a semiconductor parameter analyzer (HP 4156C, 33220s, Agilent) and a vacuum probe station (Hewlett-Packard Co. HP 4145B (Keysight)), respectively. NAND and NOR logic circuit performance was measured by using a triple output dc-power supply (E3631A, Keysight Company) to supply the input voltage (V_{IN}), with the output voltage (V_{OUT}) recorded by the semiconductor parameter analyzer.

3. Results

Understanding the internal composition of the HIZO compound is vital for evaluating its structural and chemical properties. In this regard, XPS analysis was performed using a standard Al $K\alpha$ source over a binding energy range of 0 to 1400 eV to determine the oxidation states of Hf, In, Zn, and O in the HIZO thin film. The XPS data presented in this study were calibrated using the adventitious carbon (AdC) C 1s peak at 284.6 eV, following common practice in XPS analysis. However, recent literature by Greczynski and Hultman highlights significant uncertainties associated with this conventional approach [23]. Specifically, referencing binding energies using AdC introduces inaccuracies due to the unknown and variable chemical nature of the carbon contamination layers, the lack of a stable electrical contact between the carbon layer and underlying materials, and variability in the C 1s peak position depending on the substrate's work function.

Given these critical considerations, we re-evaluated our binding energy referencing strategy by cross-verifying binding energy values against well-characterized oxide peaks inherently present in our thin-film samples, such as Zn 2p (1022.38 eV for Zn $2p_{3/2}$), In 3d (445.08 eV for In $3d_{5/2}$), and Hf 4f (18.3 eV for Hf $4f_{7/2}$), aligning these values with reported literature. This referencing helped in validation and ensured accuracy and reliability in identifying chemical states and oxidation conditions of the HIZO films. This approach effectively mitigates some of the uncertainties introduced by AdC referencing. Nevertheless, it is essential to acknowledge potential binding energy shifts and intrinsic uncertainties remaining from the original calibration method.

The high-resolution XPS spectrum of Zn 2p is depicted in Fig. 2(a). Two distinct peaks were observed at binding energies of 1022.38 eV and 1045.48 eV, which correspond to the Zn $2p_{3/2}$ and Zn $2p_{1/2}$ states, respectively. These peaks indicate a spin-orbit splitting of 23.1 eV. The positions of these peaks and the measured spin-orbit splitting are consistent with the chemical states associated with Zn-containing compounds such as ZnO, ZnS, or even elemental Zn. This characterization confirms the presence of Zn in the HIZO film, providing insights into its oxidation state and bonding environment [24,25].

Fig. 2(b) shows high resolution spectra of oxygen 1s (O 1s) for HIZO film. The spectrum reveal two primary peaks at 530.38 eV (peak 1) and 532.28 eV (peak 2), which are de-convoluted into distinct components. The peak at ≈ 530.4 corresponds to metal oxide (M–O) bonding, indicating presence of Hf, In, or Zn within the HIZO matrix [26,27]. The second peak at 532.28 is attributed to hydroxyl groups (O–H), suggesting presence of surface adsorbed hydroxides or chemisorbed water. The prominence of the hydroxyl peak may arise from exposure to ambient atmospheric conditions post-deposition or residual water vapor during processing. This observation underscores the need for controlled processing environments to minimize moisture incorporation. Despite this, the strong M–O peak confirms the formation of stable oxide bonds, supporting the integrity of the HIZO structure [28,29].

The high-resolution XPS spectra of In (In 3d) are shown in Fig. 2(c). Two main peaks are observed at binding energies of approximately 445.08 eV and 452.68 eV, corresponding to the In $3d_{5/2}$ and In $3d_{3/2}$ spin-orbit components, respectively. These peaks exhibit a spin-orbit splitting of 7.6 eV, which is consistent with indium in the +3 oxidation state, primarily found in In_2O_3 . Deconvolution of these peaks reveals additional minor components, suggesting the presence of multiple bonding environments, including potential contributions from hydroxyl groups or chemisorbed species. The dominant peaks, however, confirm the primary oxidation state of indium as +3, indicative of a stable oxide matrix. The relative intensities of the deconvoluted peaks suggest a significant contribution from the oxide form, with minor peaks attributed to surface hydroxylation. This analysis highlights the chemical stability of indium within the HIZO matrix. These findings further corroborate the presence of strong metal-oxide bonds in HIZO compound [25–27].

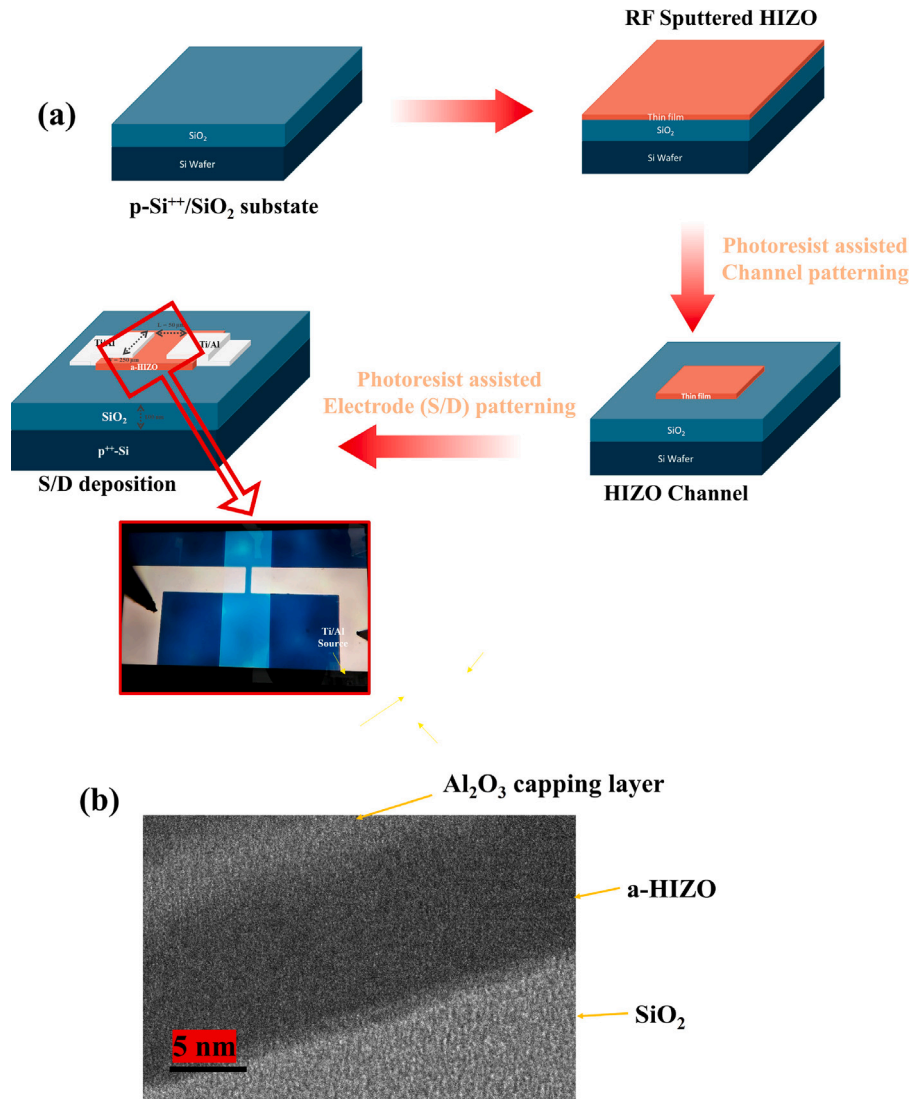


Fig. 1. (a) Fabrication process flow of HIZO TFTs showing sequential steps: RF sputtering of the HIZO channel layer, channel patterning using photoresist and UV-light exposure, and subsequent source and drain electrode deposition. The red-encircled optical image highlights the a-HIZO channel layer with the source and drain terminals, formed on a SiO_2 gate insulator over a $\text{p}^{++}\text{-Si}$ substrate. (b) Cross-sectional TEM image of the controlled sample, illustrating the a-HIZO layer (approximately 10 nm thick) deposited during a 10-min RF sputtering process on the SiO_2 gate insulator, followed by an Al_2O_3 capping layer for surface protection.

The high-resolution XPS spectra of hafnium (Hf 4f and Hf 4d) are presented in Fig. 2(d) and (e). The Hf 4f spectrum shows two primary peaks at binding energies of approximately 18.3 eV and 18.9 eV, corresponding to the Hf 4f_{7/2} and Hf 4f_{5/2} states, respectively. These peaks exhibit a spin-orbit splitting of 0.7 eV. Shifting of peaks towards higher binding energy can be due to surface hydroxides arising from atmospheric exposure. Further, the Hf 4d spectrum, shown in Fig. 2(e), supports the presence of Hf in the +4 oxidation state. Peaks are observed at approximately 213.5 eV and 224.7 eV, corresponding to the Hf 4d_{5/2} and Hf 4d_{3/2} states, respectively, with a spin-orbit splitting of 11.2 eV. These results confirm the chemical stability of Hf within the HIZO matrix [30,31].

To validate the amorphous nature and elemental homogeneity of the HIZO thin films, we performed detailed cross-sectional HRTEM and STEM-EDX elemental mapping. Fig. 3(a) presents the HRTEM image of the a-HIZO film deposited on a thermally oxidized $\text{SiO}_2/\text{p}^{++}\text{Si}$ substrate. The image series, progressing from low to high magnification, reveals a featureless contrast throughout the HIZO layer, with no distinct lattice fringes even at high magnification, confirming the absence of crystallinity. This indicates that the HIZO film is fully amorphous, consistent with the low-temperature deposition conditions employed.

To complement the HRTEM results, XRD analysis was conducted and is shown in the inset of Fig. 3(a). The XRD spectrum exhibits a broad hump centered around 25–35 °C and lacks any sharp diffraction peaks, further corroborating the amorphous nature of the HIZO thin films. These findings collectively affirm that the as-deposited HIZO channel layer is amorphous, consistent with expectations for low-temperature sputtered oxide semiconductors. The lack of any electron diffraction spots indicates that the HIZO thin film remains fully amorphous under the sputtering and post-deposition annealing conditions employed. Importantly, the incorporation of Hf into the In–Zn–O matrix does not induce crystallization or secondary phase formation (such as HfO_2). Instead, Hf appears to be well integrated into the disordered structure, likely raising the crystallization temperature and helping to stabilize the amorphous phase.

To assess the spatial distribution of the constituent elements, STEM-EDX mapping was conducted on the same sample. Fig. 3(b) displays the scanning image used for mapping, while Fig. 3(c–f) show the corresponding elemental maps for O, Zn, In, and Hf, respectively. The results confirm a homogeneous distribution of all four elements throughout the HIZO film thickness. In particular, the even distribution of oxygen is critical for ensuring stoichiometric integrity and stable oxide formation, which are essential for the reliable electrical performance of the

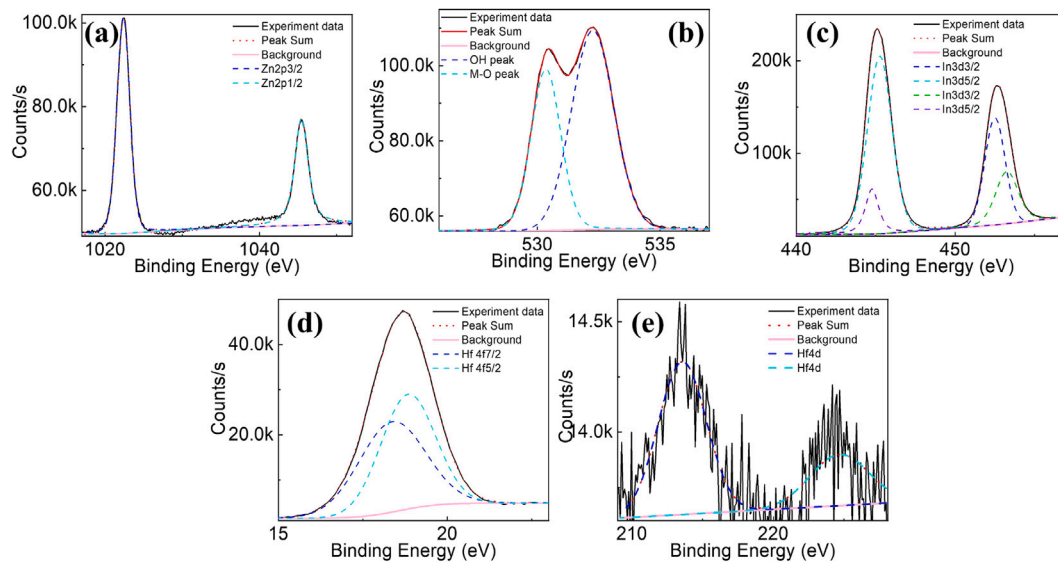


Fig. 2. High-resolution XPS spectra of the HIZO thin film. (a) Zn 2p core-level spectrum showing peaks at 1022.38 eV and 1045.48 eV corresponding to Zn 2p_{3/2} and Zn 2p_{1/2} states. (b) O 1s spectrum de-convoluted into peaks at 530.38 eV (M–O bonding) and 532.28 eV (hydroxyl groups). (c) In 3d core-level spectrum with peaks at 445.08 eV and 452.68 eV corresponding to In 3d_{5/2} and In 3d_{3/2} states, confirming the +3 oxidation state. (d) Hf 4f spectrum showing peaks at 18.3 eV and 18.9 eV corresponding to Hf 4f_{7/2} and Hf 4f_{5/2} states, indicating a +4 oxidation state. (e) Hf 4d spectrum with peaks at 213.5 eV and 224.7 eV, further supporting the +4 oxidation state of Hf. These results validate the chemical stability and bonding environments of Zn, O, In, and Hf in the HIZO matrix.

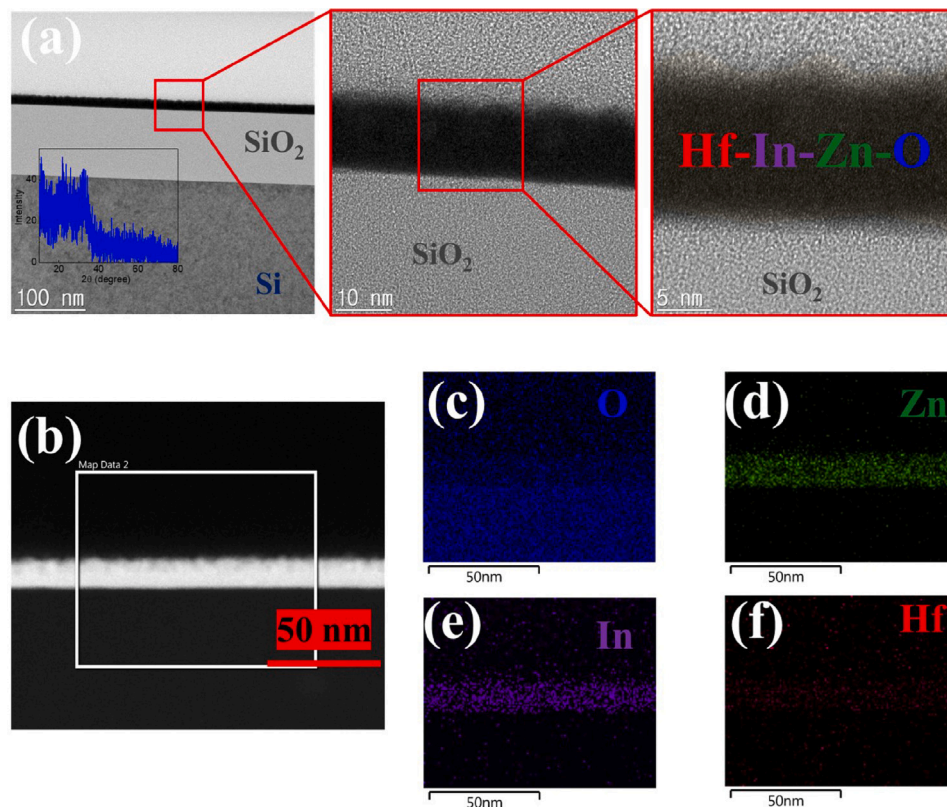


Fig. 3. (a) Cross-sectional HRTEM images of the a-HIZO thin film deposited on SiO₂/p⁺⁺ Si substrate at increasing magnifications. No lattice fringes are observed, indicating the amorphous nature of the film. The inset shows the XRD pattern exhibiting a broad hump characteristic of amorphous materials. (b) STEM image of the HIZO cross-section used for EDX mapping. Elemental maps showing the spatial distribution of (c) O, (d) Zn, (e) In, and (f) Hf. The elemental maps show that O, Zn, In, and Hf are uniformly distributed throughout the HIZO film thickness, with no evidence of phase segregation or clustering. All elements are confined to the deposited HIZO layer, demonstrating a homogeneous single-phase amorphous oxide.

resulting thin-film transistors. The oxygen map (Fig. 3(c)) exhibits a uniform intensity within the HIZO film, with a clear demarcation at the SiO₂ interface. The maps for Zn, In, and Hf (Fig. 3(d–f)) each closely overlap the same region, indicating that Zn, In, and Hf are co-localized

in the film without any concentration gradients or segregated clusters. Notably, the Hf signal is spread evenly within the HIZO layer, confirming that Hf is incorporated substitutionally or interstitially in the amorphous oxide matrix rather than forming separate Hf-rich phases.

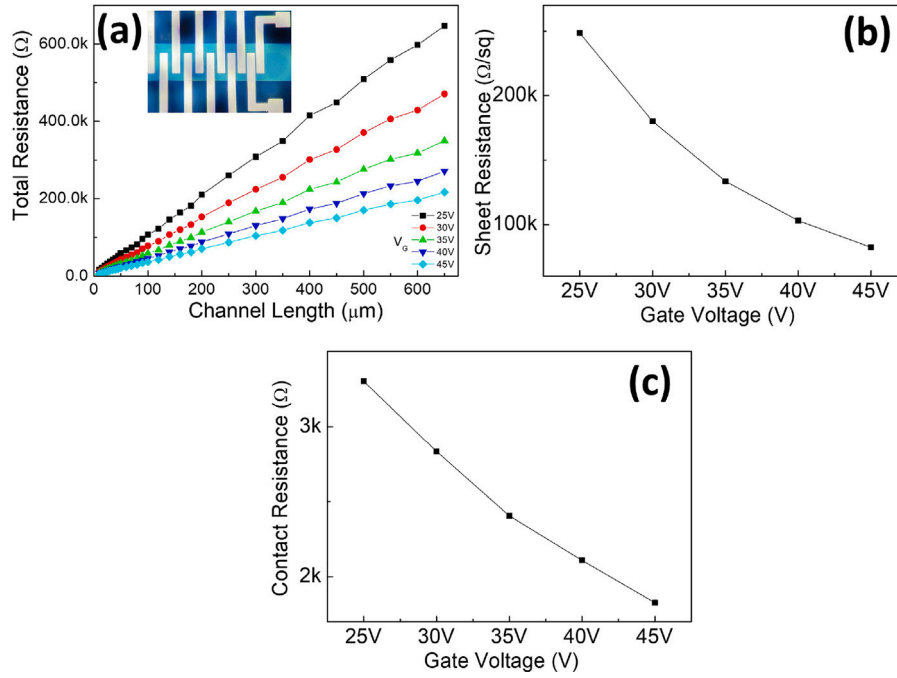


Fig. 4. (a) The total resistance as a function of the channel length with varying gate voltage. Linear change in total resistance with change in channel length suggests ohmic behavior of metal semiconductor contact. Inset shows optical image of the TLM (b) Extracted sheet resistance and (c) contact resistance with varying gate voltage. The sheet resistance and contact resistance decreases with increasing gate voltage.

In addition, the sharp drop-off of the Hf, In, and Zn signals at the HIZO/SiO₂ interface confirms that the sputtered film is well-confined to the substrate surface and that there is no unintended diffusion of metal species into the gate dielectric. The combined HRTEM and STEM-EDX data strongly support the uniform amorphous microstructure and compositional homogeneity of the HIZO thin films, consistent with the proposed model of a stable, disordered multicomponent oxide system.

The operation of the channel layer requires an ohmic contact between the semiconducting channel and the source/drain metal contacts. To optimize the performance of AOS TFTs, it is crucial to understand their electrical characteristics. In this regard, the Transmission Line Method (TLM) is a powerful tool that provides essential insights. Therefore, TLM analysis was performed to calculate the total resistance (R_{tot}), sheet resistance (R_{sh}), and contact resistance (R_c), facilitating the optimization of AOS TFT performance for various applications. Fig. 4(a) illustrates the variation in total resistance of the a-HIZO channel with changing channel length, which ranged from 10 μm to 650 μm. Inset of Fig. 4(a) shows optical image of TLM. The gate voltage was varied between 25 V and 45 V. The total resistance was extracted from the ohmic (linear) regime of the output curve (V_{drain} vs. I_{drain}) using the following equation [32,33]:

$$R_{tot} = 2R_c + \frac{R_{sh}}{W} \cdot L_{ch} \quad (1)$$

In this equation, L_{ch} represents the electrode separation, and W denotes the fixed channel width of 250 μm. R_c corresponds to the contact resistance, while R_{sh} signifies the sheet resistance of the semiconducting layer. The contact resistance is determined from the intercept ($2R_c$) of y-axis and the sheet resistance is calculated from the slope (R_{sh}/W) of the linear curve. With increasing gate voltage, the device transitions into a more conductive state, where the total resistance decreases due to the combined effects of the reduced channel resistance and lower contact resistance as shown in Fig. 4(b) and (c). The contact resistance decreased from approximately $3.3 \times 10^3 \Omega$ at a gate voltage of 25 V to $1.8 \times 10^3 \Omega$ at 45 V. Simultaneously, the sheet resistance dropped from approximately $2.5 \times 10^5 \Omega/\text{sq}$ at 25 V to $8.2 \times 10^4 \Omega/\text{sq}$ at 45 V. This improved control over the channel enables more efficient current flow between the source and drain.

Fig. 5(a) shows the I_{DS} vs. V_{GS} transfer curves of two a-HIZO TFTs. Thickness of the a-HIZO channel was 10 nm (TFT1) and 18 nm (TFT2). Transfer curve shows that the threshold voltage shifts to negative direction with increasing channel thickness. The combination of increased carrier density [34,35] and reduced effect of surface roughness in thicker channel [36] lead to the negative shift in the threshold voltage with increasing channel thickness [37]. The threshold voltage was extracted by extrapolating the linear region of the $I_{ds}^{0.5}$ vs. V_{gs} plot. Meanwhile, the field effect mobility at $V_{ds} = 5.1$ V was calculated using the following equation [38–40]:

$$\mu_{FE} = \frac{Lg_m}{WV_{ds}C_{ox}} \quad (2)$$

where g_m is transconductance, C_{ox} is capacitance of the oxide gate electrode, and L and W are channel length and width, respectively. The field effect mobility (μ_{FE}) of TFT1 and TFT2 was approximately $9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $13.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. Increased mobility in thicker channel can be attributed to the reduced effect of surface roughness on the carrier mobility as the carrier transport layer is relatively farther from the surface [36]. Further, sub-threshold swing (SS) values were calculated using following equation:

$$SS = \frac{dV_{gs}}{d(\log I_{ds})} \quad (3)$$

As increasing channel thickness, SS value slightly degraded from $0.512 \text{ V decade}^{-1}$ to $0.578 \text{ V decade}^{-1}$. Degradation in SS value can be correlated to increase in total trap density (N_{tot}). N_t is combination of bulk trap density (N_{bulk}) and interface trap density (D_{it}). N_{tot} can be calculated from using SS values as shown in following equation [41]:

$$N_{tot} = N_{bulk} + D_{it} = \left[\frac{SS \log(e)}{kT/q} - 1 \right] \frac{C_{ox}}{q} \quad (4)$$

where SS is the subthreshold swing, kT represents the thermal energy, q is the electronic charge, and C_{ox} is the dielectric capacitance of the oxide gate electrode. The calculated total trap density for TFT1 and TFT2 is approximately $1.65 \times 10^{12} \text{ cm}^{-2}$ and $1.87 \times 10^{12} \text{ cm}^{-2}$, respectively. All electrical parameters, including threshold voltage, on/off current ratio (I_{on}/I_{off}), field-effect mobility, SS value, and total

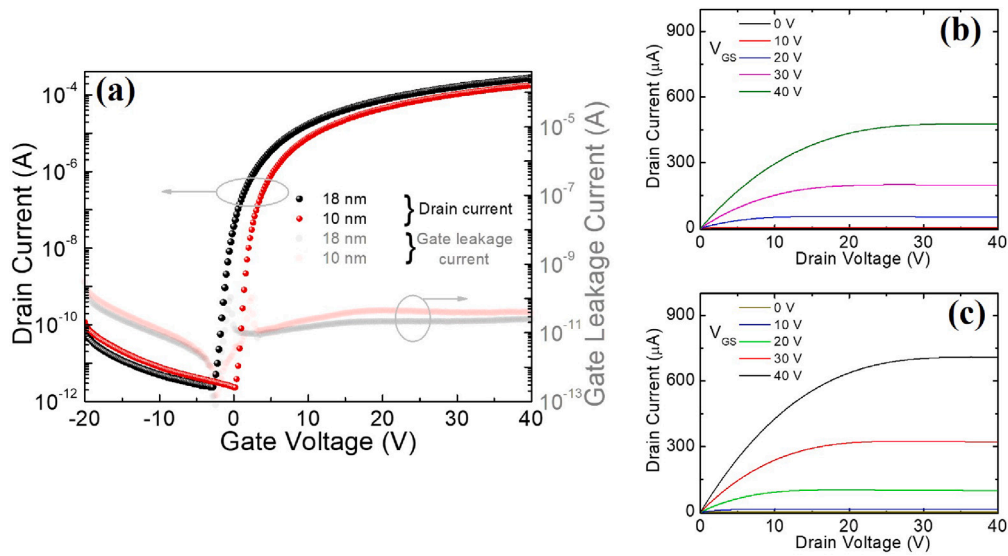


Fig. 5. (a) Transfer characteristic of TFT1 and TFT2. Output curve of (b) TFT1 and (c) TFT2.

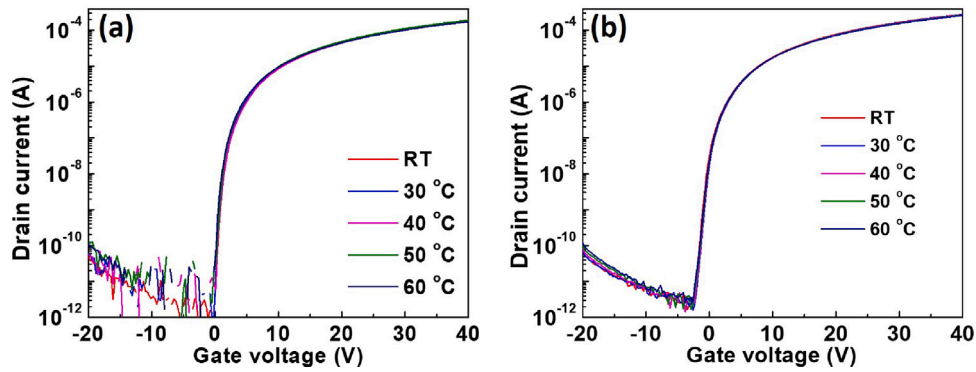


Fig. 6. Transfer characteristics of (a) TFT1 and (b) TFT2 under temperature stress. The absence of changes in the transfer characteristics with increasing temperature signifies highly stable devices.

Table 1

Extracted device parameters of some selected amorphous a-HIZO thin film transistors TFTs with different thicknesses.

a-HIZO	μ_{FE} ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	V_{th} (V)	I_{on}/I_{off}	SS (V decade ⁻¹)	N_{tot} ($\times 10^{12} \text{cm}^{-2}$)
10 min	9.12	3.13	7.78×10^7	0.512	1.65
18 min	13.48	1.15	1.17×10^8	0.578	1.87

trap density, are summarized in Table 1. Fig. 5(b) and (c) show the typical output characteristics (V_{ds} vs. I_{ds}) of TFT1 and TFT2. TFT2 exhibits increased drain current compared to TFT1 for the same gate voltage. This increased drain current corresponds to the higher mobility observed in TFT2.

The temperature stability of both devices was tested under vacuum conditions using a vacuum probe station. This setup was chosen to eliminate the effects of adsorption and desorption of water molecules and/or oxygen from the ambient environment. The devices were subjected to temperature stress up to 60 °C, starting from room temperature (RT). Transfer characteristics were measured at RT, 30 °C, 40 °C, 50 °C, and 60 °C. Fig. 6(a) and (b) show the transfer characteristics of TFT1 and TFT2 under temperature stress, respectively. Both TFTs exhibited no discernible change in their transfer characteristics, demonstrating very stable device performance.

Table 2 presents a summary of some of the reported amorphous HIZO TFTs from the literature. As shown, HIZO TFTs can achieve

Table 2

Performance summary of reported a-HIZO TFTs from the literature.

a-HIZO	μ_{FE} ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	I_{on}/I_{off}	SS (V decade ⁻¹)	Process Temp °C
HIZO [42]	1.94	10^6	0.58	500
HIZO [22]	≈ 8	10^8	≈ 0.17	150
HIZO [43]	5.35	10^8	0.35	300
HIZO [44]	18.1	10^7	0.4	400
HIZO [45]	4.7	10^8	0.55	250
HIZO [19]	10	10^8	0.23	200
HIZO ^{This work}	13.48	10^8	0.58	150

high mobility (10–30 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$), steep subthreshold slopes (< 0.6 V/dec), and a large on/off ratio across various processing temperatures. The HIZO TFTs in our work show excellent electrical properties while being fabricated at a lower temperature (150 °C), confirming their superior charge transport characteristics. However, the main novelty of our study is the integration of these HIZO devices into logic circuits, leveraging the material's high intrinsic mobility and stability to realize functional inverters and logic gates for the first time using HIZO TFTs.

Fig. 7(a) illustrates the schematic of the equivalent circuit for an NMOS inverter, utilizing a saturated depletion (D)-mode TFT as the active load or pull-up device. This depletion-load-type inverter was constructed using two TFTs with differing threshold voltages. The D-mode TFT, serving as the load device, has a threshold voltage that is negative relative to the E-mode TFT. In the D-mode TFT, the gate

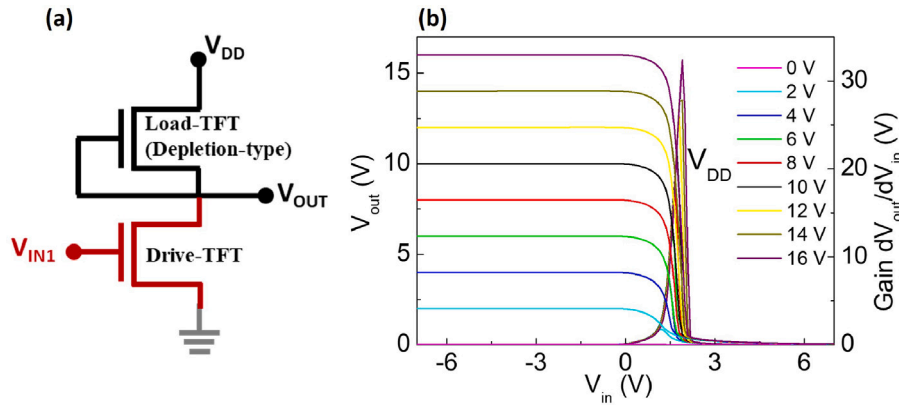


Fig. 7. (a) schematic of the equivalent circuit for an NMOS inverter, utilizing a saturated depletion (D)-mode TFT. (b) VTC characteristics and voltage gain of depletion-load type inverter obtained for supply voltage from 2 to 16 V.

Table 3

Calculated maximum gain values for supply voltage ranging from 2 V to 16 V.

V_{dd}	2 V	4 V	6 V	8 V	10 V	12 V	14 V	16 V
Voltage gain	1.77	7.77	13.22	17.80	22.16	25.91	27.78	32.38

and source terminals are connected, ensuring that the device remains 'ON' regardless of the input voltage (V_{in}). Fig. 7(b) shows the typical voltage transfer characteristics (VTC) of the inverter composed of a TFT1 and TFT2 with supply voltage V_{dd} ranging from 0 V to 16 V in 2 V increments. In this depletion-type inverter, TFT2 acts as the load-TFT and TFT1 as drive-TFT. When V_{in} is 0 V, the output voltage (V_{out}) is nearly equal to the supply voltage V_{dd} . As V_{in} further increases, the drive TFT switches 'ON', leading to a drop in V_{out} to 0 V once the inverter's threshold voltage is surpassed. The inverter's response was observed across a voltage range from -7 V (low voltage) to +7 V (high voltage). When V_{in} is -7 V (logic 0), the load transistor is 'ON' and drive transistor is 'OFF', resulting in V_{out} being close to V_{DD} (logic 1). Conversely, when V_{in} is +7 V (logic 1), both the load transistor and the drive transistor are 'ON', resulting in V_{out} being close to 0 V (logic 0). Thus, incorporating TFT1 and TFT2 achieves a full swing logic inverter. For an inverter, the voltage gain, which is defined as dV_{out}/dV_{in} , serves as an essential benchmark for evaluating the quality of inverters fabricated using TFTs. Table 3 presents the maximum voltage gain of inverters for various V_{dd} . A maximum gain of 32.38 was calculated for $V_{dd} = 16$ V. These voltage gains are comparable to some of reported a-IGZO, a-SZTO, a-SIZO, ITO (tin doped indium oxide), and SnO_2 based inverters [17,18,39,46,47]. To the best of our knowledge, this is the first report based on a-HIZO-based inverter achieving a gain of approximately 32.

To further explore the potential of a-HIZO TFTs, more complex logic circuits such as NOR and NAND gates were also implemented. The NOR gate was constructed with two parallel drive transistors (TFT1) connected to a load transistor (TFT2), while the NAND gate was created using a series connection of two drive transistors (TFT1) with a load transistor (TFT2). Fig. 8(a) and (c) illustrate the schematic diagrams and truth tables for the NOR and NAND gates, respectively. The performance of these gates was evaluated using a fixed V_{dd} of 10 V, with the input signals (V_{in}) of +10 V representing a logic '1' (high) and -10 V representing a logic '0' (low). Each gate had two input terminals (V_{IN1} and V_{IN2}) for the drive transistors and one output terminal (V_{OUT}). For the NOR logic gate, V_{OUT} is 10 V ('1' high) when both inputs are at -10 V ('0' low). The output drops to 0 V ('0' low) when either or both of the input are at +10 V ('1' high), as shown in Fig. 8(b). Conversely, for the NAND logic gate, V_{OUT} remains at 10 V ('1' high) when both inputs or any one of the inputs are at -10 V ('0' low). The output drops to 0 V ('0' low) only when both inputs are at +10 V ('1' high), as shown in Fig. 8(d). These measurements confirm the formation of NOR and NAND logic circuits using a-HIZO TFTs.

4. Conclusion

In summary, we fabricated and characterized high-performance a-HIZO thin-film transistors (TFTs) and demonstrated their integration into full-swing inverters and logic circuits. Structural characterization using cross-sectional HRTEM and XRD confirmed the fully amorphous nature of the HIZO films. STEM-EDX elemental mapping validated the homogeneous distribution of Hf, In, Zn, and O across the film, supporting the proposed model of a stable, single-phase multicomponent oxide. XPS analysis confirmed the stable oxidation states of all constituent elements and highlighted the chemical stability of the amorphous oxide matrix. The fabricated a-HIZO TFTs exhibited a maximum field-effect mobility of approximately $13.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on-off ratio of 10^8 and SS value ranging from 0.5 to 0.6 V decade⁻¹. Additionally, a temperature stress test was conducted to assess the stability of the a-HIZO TFTs, demonstrating that the devices remained highly stable even at 60 °C. A full-swing depletion-type logic inverter fabricated using a-HIZO TFTs achieved a high voltage gain of 32.38. Furthermore, the development of NOR and NAND logic gates showcased the scalability and applicability of these devices for advanced electronic circuits. These results establish a-HIZO TFTs as promising candidates for next-generation low-power and high-performance integrated electronics.

CRedit authorship contribution statement

Sandeep Kumar Maurya: Writing – review & editing, Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Eun Ji Yang:** Writing – review & editing, Writing – original draft, Investigation, Data curation. **Sang Yeol Lee:** Writing – review & editing, Validation, Supervision, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

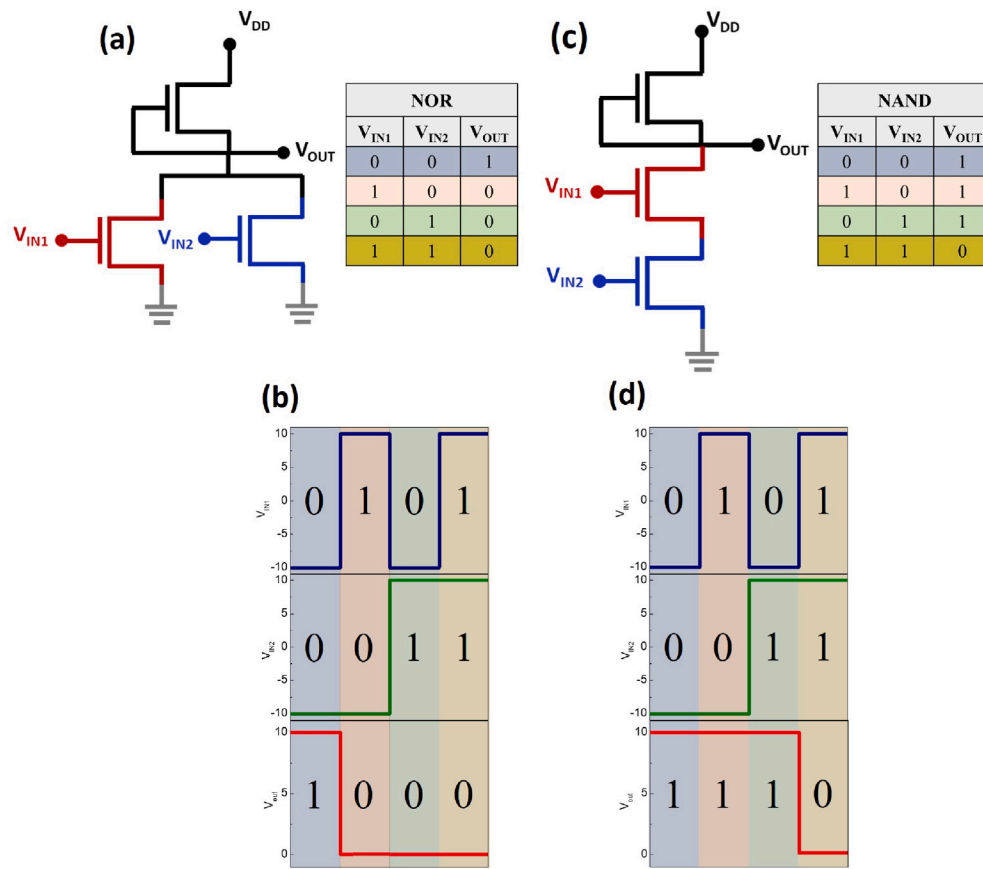


Fig. 8. Schematic diagrams and truth tables for the (a) NOR and (b) NAND gates. Truth table verification of (b) NOR gate and (d) NAND gate.

References

- [1] P.G. Carey, P.M. Smith, S.D. Theiss, P. Wickboldt, Polysilicon thin film transistors fabricated on low temperature plastic substrates, *J. Vac. Sci. Technol. A: Vac. Surf. Films* 17 (4) (1999) 1946–1949.
- [2] C.-S. Yang, L. Smith, C. Arthur, G. Parsons, Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates, *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. Process. Meas. Phenom.* 18 (2) (2000) 683–689.
- [3] S.-C. Wang, C.-F. Yeh, C.-K. Huang, Y.-T. Dai, Device transfer technology by backside etching (DTBE) for poly-Si thin-film transistors on glass/plastic substrate, *Japan. J. Appl. Phys.* 42 (9A) (2003) L1044.
- [4] H. Hosono, M. Yasukawa, H. Kawazoe, Novel oxide amorphous semiconductors: Transparent conducting amorphous oxides, *J. Non-Cryst. Solids* 203 (1996) 334–344.
- [5] E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: a review of recent advances, *Adv. Mater.* 24 (22) (2012) 2945–2986.
- [6] S.Y. Lee, Comprehensive review on amorphous oxide semiconductor thin film transistor, *Trans. Electr. Electron. Mater.* 21 (2020) 235–248.
- [7] A. Liu, H. Zhu, W.-T. Park, S.-J. Kim, H. Kim, M.-G. Kim, Y.-Y. Noh, High-performance p-channel transistors with transparent Zn doped-CuI, *Nat. Commun.* 11 (1) (2020) 4309.
- [8] D. Dhananjay, C.-W. Chu, C.-W. Ou, M.-C. Wu, Z.-Y. Ho, K.-C. Ho, S.-W. Lee, Complementary inverter circuits based on p-SnO₂ and n-In₂O₃ thin film transistors, *Appl. Phys. Lett.* 92 (23) (2008).
- [9] A. Dindar, J. Kim, C. Fuentes-Hernandez, B. Kippelen, Metal-oxide complementary inverters with a vertical geometry fabricated on flexible substrates, *Appl. Phys. Lett.* 99 (17) (2011).
- [10] H. Chang, C.-H. Huang, K. Matsuzaki, K. Nomura, Back-channel defect termination by sulfur for p-channel Cu₂O thin-film transistors, *ACS Appl. Mater. Interfaces* 12 (46) (2020) 51581–51588.
- [11] S.-M. Hsu, D.-Y. Su, F.-Y. Tsai, J.-Z. Chen, I.-C. Cheng, Flexible complementary oxide thin-film transistor-based inverter with high gain, *IEEE Trans. Electron Devices* 68 (3) (2021) 1070–1074.
- [12] M. Ofuji, K. Abe, H. Shimizu, N. Kaji, R. Hayashi, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, H. Hosono, Fast thin-film transistor circuits based on amorphous oxide semiconductor, *IEEE Electron Device Lett.* 28 (4) (2007) 273–275.
- [13] K. Nomura, Recent progress of oxide-TFT-based inverter technology, *J. Inf. Disp.* 22 (4) (2021) 211–229.
- [14] M. Elsobky, M. Elattar, G. Alavi, F. Letzkus, H. Richter, U. Zschieschang, M. Strecker, H. Klauk, J.N. Burghartz, A digital library for a flexible low-voltage organic thin-film transistor technology, *Org. Electron.* 50 (2017) 491–498.
- [15] S. Han, S.Y. Lee, High performance of full swing logic inverter using all n-types amorphous ZnSnO and SiZnSnO thin film transistors, *Appl. Phys. Lett.* 106 (21) (2015).
- [16] J.-M. Lee, I.-T. Cho, J.-H. Lee, H.-I. Kwon, Full-swing InGaZnO thin film transistor inverter with depletion load, *Japan. J. Appl. Phys.* 48 (10R) (2009) 100202.
- [17] M. Wang, L. Liang, H. Luo, S. Zhang, H. Zhang, K. Javadi, H. Cao, Threshold voltage tuning in a-IGZO TFTs with ultrathin SnO_x capping layer and application to depletion-load inverter, *IEEE Electron Device Lett.* 37 (4) (2016) 422–425.
- [18] B.H. Lee, K.-S. Cho, A. Sohn, S. Hwang, S.Y. Lee, Electrode-adaptive thin-film integrated logic circuits, *IEEE Trans. Electron Devices* 66 (2) (2019) 957–962.
- [19] C.-J. Kim, S. Kim, J.-H. Lee, J.-S. Park, S. Kim, J. Park, E. Lee, J. Lee, Y. Park, J.H. Kim, et al., Amorphous hafnium-indium-zinc oxide semiconductor thin film transistors, *Appl. Phys. Lett.* 95 (25) (2009).
- [20] H.-S. Kim, K.-B. Park, K.S. Son, J.S. Park, W.-J. Maeng, T.S. Kim, K.-H. Lee, E.S. Kim, J. Lee, J. Suh, et al., The influence of sputtering power and O₂/Ar flow ratio on the performance and stability of Hf-In-Zn-O thin film transistors under illumination, *Appl. Phys. Lett.* 97 (10) (2010).
- [21] Y.-G. Mo, M. Kim, K.S. Kim, C.M. Park, Y.S. Park, C.G. Choi, K. Uh, S. Kim, 35.1: 14-inch AMOLED TV Driven by HfInZnO Thin-Film Transistors, in: *SID Symposium Digest of Technical Papers*, vol. 42, Wiley Online Library, 2011, pp. 472–475, 1.
- [22] C.-H. Ho, D.-S. Tsai, C. Lu, S.Y. Kim, S. Mungan, S.-G. Yang, Y. Zhang, J.-H. He, Device process and circuit application interaction for harsh electronics: Hf-In-Zn-O thin film transistors as an example, *IEEE Electron Device Lett.* 38 (8) (2017) 1039–1042.
- [23] G. Greczynski, L. Hultman, Binding energy referencing in X-ray photoelectron spectroscopy, *Nat. Rev. Mater.* 10 (1) (2025) 62–78.
- [24] D. Goyal, C. Agashe, M. Takwale, V. Bhide, S. Mahamuni, S. Kulkarni, Dopant induced modifications in the physical properties of sprayed ZnO: In films, *J. Mater. Res.* 8 (5) (1993) 1052–1056.
- [25] Y.R. Denny, H.C. Shin, S. Seo, S.K. Oh, H.J. Kang, D. Tahir, S. Heo, J.G. Chung, J.C. Lee, S. Tougaard, Electronic and optical properties of hafnium indium zinc oxide thin film by XPS and REELS, *J. Electron Spectrosc. Relat. Phenom.* 185 (1–2) (2012) 18–22.

- [26] X. Chen, J. Peng, C. Hao, J. Ji, Z. Huo, et al., Transparent and conductive IZO films: Oxygen and discharge voltage controlled sputtering growth and properties, *Vacuum* 195 (2022) 110645.
- [27] S. Zhang, L. Weng, B. Liu, D. Kuang, X. Liu, B. Jiang, G. Zhang, Z. Bao, G. Yuan, J. Guo, et al., The improved properties of solution-based InGaSnO (IGTO) thin film transistor using the modification of InZnO (IZO) layer, *Vacuum* 215 (2023) 112225.
- [28] M. Kundu, T. Hasegawa, K. Terabe, K. Yamamoto, M. Aono, Structural studies of copper sulfide films: effect of ambient atmosphere, *Sci. Technol. Adv. Mater.* 9 (3) (2008) 035011.
- [29] M.C. Biesinger, L.W. Lau, A.R. Gerson, R.S.C. Smart, Resolving surface chemical states in XPS analysis of first row transition metals, oxides and hydroxides: Sc, Ti, V, Cu and Zn, *Appl. Surf. Sci.* 257 (3) (2010) 887–898.
- [30] C.-H. Li, J.-Z. Chen, Electrical, optical, and microstructural properties of sol-gel derived HfZnO thin films, *J. Alloys Compd.* 601 (2014) 223–230.
- [31] S. Hong, S.P. Park, Y.-g. Kim, B.H. Kang, J.W. Na, H.J. Kim, Low-temperature fabrication of an HfO₂ passivation layer for amorphous indium-gallium-zinc oxide thin film transistors using a solution process, *Sci. Rep.* 7 (1) (2017) 16265.
- [32] S. Lee, H. Park, D.C. Paine, A study of the specific contact resistance and channel resistivity of amorphous IZO thin film transistors with IZO source-drain metallization, *J. Appl. Phys.* 109 (6) (2011).
- [33] S.Y. Lee, Investigation on contact resistance of amorphous indium gallium zinc oxide thin film transistors with various electrodes by transmission line method, *Trans. Electr. Electron. Mater.* 16 (3) (2015) 139–141.
- [34] H. Kim, a.C. Gilmore, A. Pique, J. Horwitz, H. Mattoussi, H. Murata, Z. Kafafi, D. Chrisey, Electrical, optical, and structural properties of indium-tin-oxide thin films for organic light-emitting devices, *J. Appl. Phys.* 86 (11) (1999) 6451–6461.
- [35] K. Ide, K. Nomura, H. Hosono, T. Kamiya, Electronic defects in amorphous oxide semiconductors: A review, *Phys. Status Solidi (A)* 216 (5) (2019) 1800372.
- [36] Y. Wang, X.W. Sun, G.K.L. Goh, H.V. Demir, H.Y. Yu, Influence of channel layer thickness on the electrical performances of inkjet-printed In-Ga-Zn oxide thin-film transistors, *IEEE Trans. Electron Devices* 58 (2) (2010) 480–485.
- [37] J. Jeong, Y. Hong, Debye length and active layer thickness-dependent performance variations of amorphous oxide-based TFTs, *IEEE Trans. Electron Devices* 59 (3) (2012) 710–714.
- [38] B.H. Lee, D.-Y. Lee, A. Sohn, S. Park, D.-W. Kim, S.Y. Lee, Direct investigation on energy bandgap of Si added ZnSnO system for stability enhancement by X-ray photoelectron spectroscopy, *J. Alloys Compd.* 715 (2017) 9–15.
- [39] B.H. Lee, S. Kim, S.Y. Lee, Investigation on dependency mechanism of inverter voltage gain on current level of photo stressed depletion mode thin-film transistors, *Solid-State Electron.* 156 (2019) 5–11.
- [40] B. Murugan, S.Y. Lee, Effects of change of oxygen vacancy on hysteresis voltage and stability under time-temperature dependence positive bias stress in amorphous SZTO transistors, *Microelectron. Eng.* 253 (2022) 111678.
- [41] D.K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, Ltd, Hoboken, New Jersey, ISBN: 9780471749097, 2005, pp. 185–250.
- [42] W.H. Jeong, G.H. Kim, H.S. Shin, B. Du Ahn, H.J. Kim, M.-K. Ryu, K.-B. Park, J.-B. Seon, S.Y. Lee, Investigating addition effect of hafnium in InZnO thin film transistors using a solution process, *Appl. Phys. Lett.* 96 (9) (2010).
- [43] J.S. Park, K.S. Son, T.S. Kim, J.S. Jung, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E.S. Kim, K.-B. Park, J.-B. Seon, et al., High performance and stability of double-gate Hf-In-Zn-O thin-film transistors under illumination, *IEEE Electron Device Lett.* 31 (9) (2010) 960–962.
- [44] Y. Gao, X. Li, L. Chen, J. Shi, X.W. Sun, J. Zhang, High Mobility Solution-Processed Hafnium Indium Zinc Oxide TFT With an Al-Doped ZrO₂ Gate Dielectric, *IEEE Electron Device Lett.* 35 (5) (2014) 554–556.
- [45] S.-I. Kim, S.W. Kim, C.J. Kim, J.-S. Park, The impact of passivation layers on the negative bias temperature illumination instability of Hf-In-Zn-O TFT, *J. Electrochem. Soc.* 158 (2) (2010) H115.
- [46] S. Hong, J.W. Na, I.S. Lee, H.T. Kim, B.H. Kang, J. Chung, H.J. Kim, Simultaneously defined semiconducting channel layer using electrohydrodynamic jet printing of a passivation layer for oxide thin-film transistors, *ACS Appl. Mater. Interfaces* 12 (35) (2020) 39705–39712.
- [47] K. Liang, H. Ren, D. Li, Y. Wang, Y. Tang, M. Zhao, H. Wang, W. Li, B. Zhu, Fully-printed flexible n-type tin oxide thin-film transistors and logic circuits, *J. Mater. Chem. C* 9 (35) (2021) 11662–11668.