



Enhancement in electrical properties of dual-active-layer amorphous SiZnSnO/SiInZnO thin film transistors[☆]

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ARTICLE INFO

Keywords:

Amorphous oxide semiconductor
Thin film transistor
Bi-layer-TFT
Field effect mobility

ABSTRACT

Bi-layer thin film transistors (TFTs) have been fabricated with a channel structure comprising a dielectric layer, a semiconducting amorphous-Si-In-Zn-O (a-SIZO) layer, and a semiconducting amorphous-Si-Zn-Sn-O (a-SZTO) layer, aiming to improve field effect mobility and stability. These films were deposited using RF sputtering at room temperature. The TFTs with a bottom gate top contact, processed at 500 °C, exhibited high mobilities ($>32 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) along with a current on/off ratio of approximately 10^8 and a subthreshold swing (SS) value below $0.5 \text{ V decade}^{-1}$ primarily because of reduced trap density and presence of highly conducting ultrathin a-SIZO layer. Furthermore, the bi-layer TFTs demonstrated notable stability under negative and positive bias temperature stress conditions.

1. Introduction

Oxide Semiconductors are some of most used materials for thin film transistors (TFTs) [1–3]. Among all oxide semiconductors, amorphous oxide semiconductors (AOS) stand out as the most promising materials for their application in various advanced display technologies, sensors, and related fields [4,5]. AOS display exceptional optical transparency, excellent uniformity, superior electrical properties, and flexibility. Room temperature fabricated AOS exhibit hall mobility similar to those of crystalline materials. High mobility in these AOS materials is due to overlap among neighboring metal *ns* orbitals. The amorphous nature, coupled with high mobility in these materials, opens up possibilities for their utilization in various flexible electronics [6]. In 2003, Nomura et al. epitaxially grown a complex $\text{InGaO}_3(\text{ZnO})_5$ (GIZO) single-crystalline semiconductor on yttria-stabilized zirconia substrate and fabricated TFT with effective mobility of $80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on/off ratio of 10^6 [7]. However, the process required temperature as high as 1400 °C to obtain a high performing TFT. Further in 2004, Nomura et al. successfully fabricated the first transparent and flexible oxide based TFT which have attracted considerable interest of lot of researchers from all over the world [8]. In comparison to amorphous Si (a-Si:H) TFT and low-temperature polysilicon (LTPS), AOS require low processing temperatures, show enhanced stability, and are compatible with innovative materials such as polymer ferromagnetic

materials. AOS is held as next-generation technology and has potential to replace Si-based Complementary Metal-Oxide-Semiconductor (CMOS) circuits [9–11].

Despite several advantages, most AOS exhibit poor stability and electrical performance. AOS performance is primarily limited by the intrinsic mobility and the limitation to efficiently turning off the device [12]. Various strategies have been explored to address these issues, including the incorporation of high-*k* insulators, in situ metal oxide capping, and the utilization of low dimensional semiconducting heterostructures [13,14]. In particular, the use of multilayers of different materials has become very interesting for its potential in enhancing the electrical performance of TFTs based on AOS. This approach could help in overcoming some of limitations associated with AOS and could lead to advancement in TFT technology. Over the last decade, numerous studies have been conducted on bi-layer channel structures, incorporating various AOS as the channel layer. These TFT show improved electrical properties with enhanced stability [15–19]. However, it is noteworthy that most of AOS-based TFTs demonstrate instability under temperature, negative bias temperature stress (NBTS), and positive bias temperature stress (PBTS). The stability under both negative and positive bias conditions is crucial for the successful application of TFTs in active-matrix organic light-emitting diodes (AMOLED) and active-matrix liquid-crystal display (AMLCD) devices [20].

[☆] The review of this paper was arranged by Sorin Cristoloveanu.

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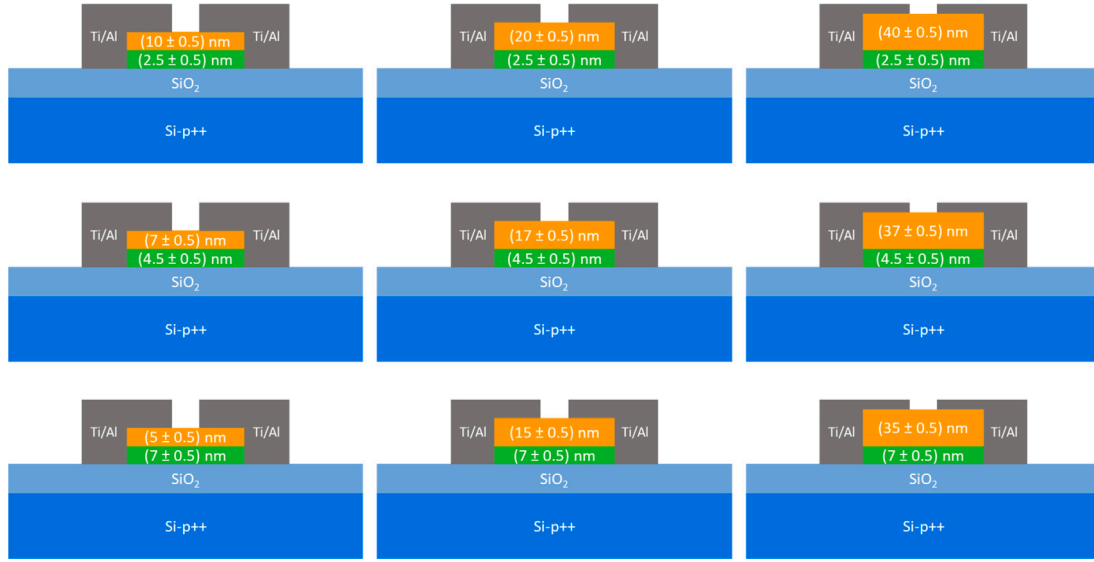


Fig. 1. Cross-sectional schematic of the bi-layer structure of the TFT devices. The thickness of the bottom SIZO layer has been varied from (2.5 ± 0.5) to (7 ± 0.5) nm. The top SZTO thickness has been adjusted to fabricate TFT devices with thicknesses of (12 ± 1) , (22 ± 1) , and (42 ± 1) nm.

The TFTs based on amorphous SiInZnO (a-1SIZO, where Si is 1% by wt in the composite material) with a bottom gate and top electrode show outstanding performance but suffers from high instability in ambient conditions. This instability is primarily attributed to the absorption of O_2 from the air on the channel surface, leading to increased trap density and subsequent degradation of the SS (sub-threshold swing) value [21]. To address this issue, we introduced a more stable amorphous SiZnSnO (a-0.5SZTO, where Si is 0.5% by wt in the composite material) passivation layer with similar electrical properties, aiming to enhance overall TFT device performance. In this study, we successfully fabricated TFTs with a heterojunction channel layer of a-SIZO/a-SZTO, demonstrating excellent electrical properties and high stability under negative and positive bias temperature tests. The bi-layer channel TFTs exhibit a maximum field-effect mobility of $> 32 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with an on/off current ratio of $> 10^8$ and operational stability in negative and positive bias stress.

2. Experimental

Bottom gate bilayer TFTs were fabricated using RF magnetron sputtering at room temperature. The devices were configured as shown in Fig. 1. The bilayer structure was created with different thicknesses of 0.5 wt % SiZnSnO (0.5SZTO) and 1 wt % SiInZnO (1SIZO). Deposition was carried out on a 100 nm $\text{SiO}_2/\text{p}^{++}\text{-Si}$ substrate, with SiO_2 serving as the gate insulator. The $\text{SiO}_2/\text{p}^{++}\text{-Si}$ substrates underwent sequential cleaning with acetone, methanol, and DI water for 10 min each in an ultrasonication bath, followed by drying with N_2 gas.

The deposition chamber's base pressure before each deposition was approximately 5×10^{-6} T. Deposition power, pressure, and Ar flow for all 0.5SZTO depositions were maintained at a constant 50 W, 6 mT, and 40 sccm, respectively. For 1SIZO films, deposition power, pressure, and Ar flow were kept constant at 60 W, 12 mT, and 40 sccm, respectively. Deposition times were varied to achieve the desired film thickness, as illustrated in Fig. 1. Three batches of devices were fabricated with bilayer channel thicknesses of (12.0 ± 1) nm, (22.0 ± 1) nm, and (42.0 ± 1) nm, corresponding to 1SIZO thicknesses of (2.5 ± 0.5) nm, (4.5 ± 0.5) nm, and (7.0 ± 0.5) nm.

After deposition of 0.5SZTO/1SIZO, the bilayer thin film underwent wet etching process to form channel with width of 250 μm and length of 50 μm . Following channel patterning, films were annealed in air at 500 $^\circ\text{C}$ for 2 h. The source and drain electrodes (S/D) were deposited

via e-beam evaporation (10 nm Ti) and thermal evaporation (40 nm Al) followed by lift-off process.

The electrical characteristics and the stability were carried out in the dark box using a semiconductor parameter analyzer (HP 4156C) and a vacuum probe station (MS Tech with HP 4145B (Keysight) analyzer), respectively. The transmittance of bi-layer film deposited on glass substrate was analyzed by UV-Vis optical spectrometer (Carry 5000 UV-Vis-NIR, Agilent). High-resolution transmission electron microscopy (TEM) images were captured using the TEM-Titan instrument.

3. Results

The device structure employed in the present study is illustrated in Fig. 2. This figure exhibits cross-sectional TEM images, including an enlarged perspective of one of the bi-layer channel layers. TEM imaging was conducted on the bi-layer channel, featuring a 1SIZO thickness of (2.5 ± 0.5) nm and a 0.5SZTO thickness of (10 ± 0.5) nm. Upon closer examination using TEM, it is evident that the SiO_2 thickness measures 100 nm. Additionally, the thickness of 1SIZO is approximately 2.54 nm, while the thickness of 0.5SZTO is measured at 10.5 nm. These findings are consistent with our deposition predictions. Further, TEM images play a dual role in not only affirming the thickness measurements but also offering a visual confirmation of the uniformity observed in the thin film deposition.

Fig. 3 shows transfer curves of bi-layer TFTs. Transfer curves were measured with varying gate to source voltage from -30 V to 30 V at constant drain to source voltage (V_{DS}) of 5.1 V. Fig. 3(a), (b), and (c) show I_{DS} versus V_{DS} curves of (12.0 ± 1) nm, (22.0 ± 1) nm, and (42.0 ± 1) nm thick 1SIZO/0.5SZTO bi-layer TFT with different thicknesses of 1SIZO and 0.5SZTO. Fig. 4(a), (b), and (c) show all extracted device parameters. For all TFTs, threshold voltage (V_{th}) decreases with increasing the thickness of 1SIZO from (2.5 ± 0.5) to (7 ± 0.5) nm and subsequent increase in OFF-current is also observed. This indicates that when the 1SIZO layer is thicker, it allows more current to flow when the device is in off state. This happens due to presence of more electrons in the E_{CB} (conduction band), making it easier for them to move. The field effect mobility was determined at $V_{DS} = 5.1 \text{ V}$ by employing following equation [22]:

$$\mu_{FE} = \frac{Lg_m}{WV_{ds}C_{ox}} \quad (1)$$

where g_m is transconductance, C_{ox} is capacitance of the oxide gate electrode, and L and W are channel length and width, respectively.

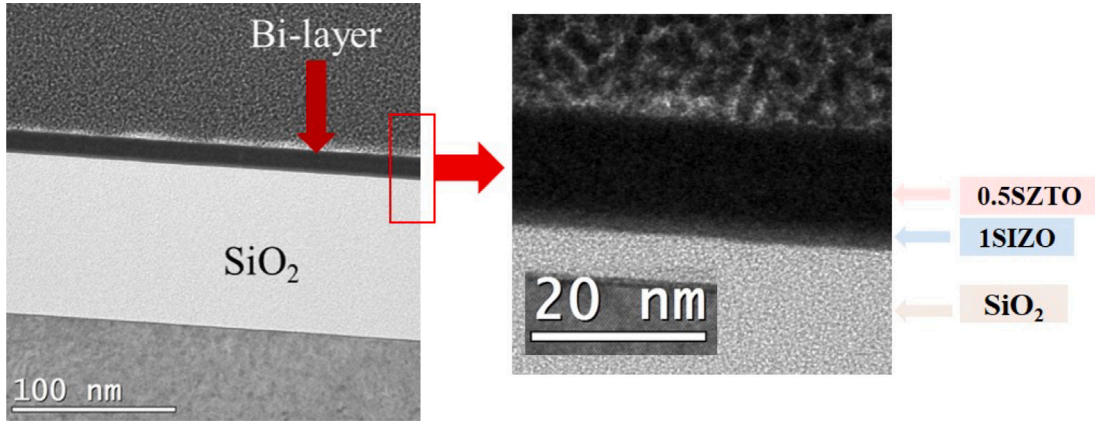


Fig. 2. Cross-section TEM image of bi-layer channel. The bi-layer consist of 1SIZO and 0.5 SZTO layer.

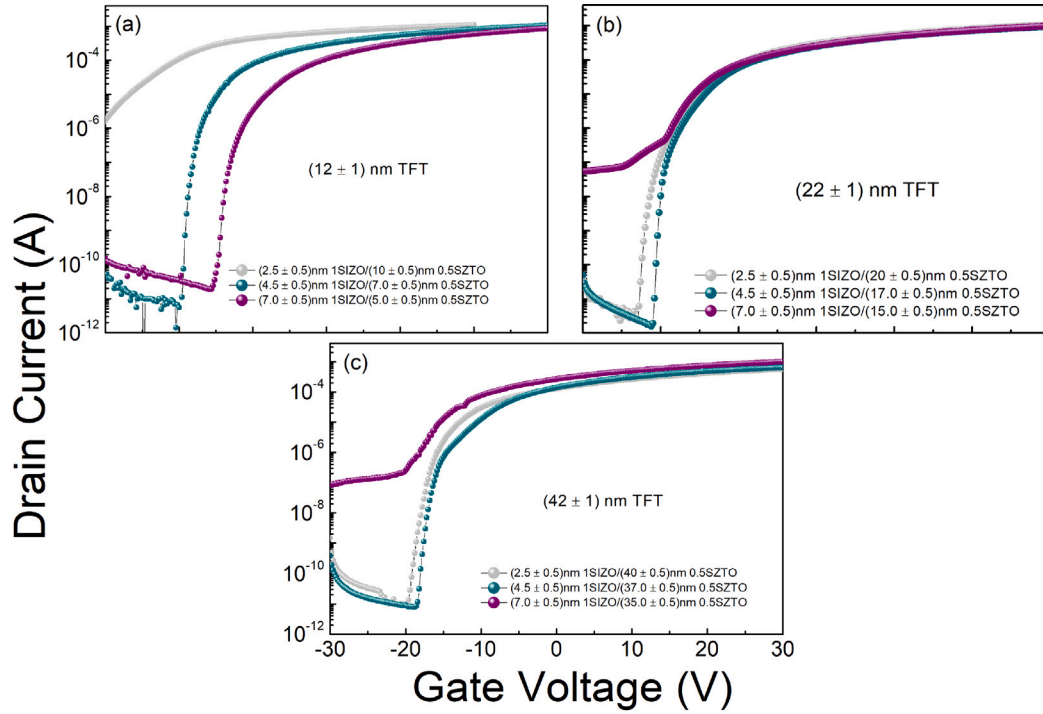


Fig. 3. Transfer characteristics of bi-layer TFTs with thickness of (a) (12 ± 1) nm, (b) (22 ± 1) nm, (c) (42 ± 1) nm. The scale on the y-axis and the x-axis remains consistent across all plots.

The field effect mobility of 0.5SZTO TFT without an 1SIZO layer was $\approx 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ as shown in supplementary Fig.S1. Whereas, the field effect mobility for bi-layer 0.5SZTO stacked with ultra thin 1SIZO layered TFT was increased to $> 30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. However, further increase in 1SZTO thickness does not improve the mobility and it saturates at $\approx 30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Furthermore, increase in 1SIZO thickness also degrades SS from 0.45 to $2.5 \text{ V decade}^{-1}$, and on/off ratio also deteriorated considerably from 10^8 to 10^4 . It is noteworthy that, an 1SIZO layer thicker than (4.5 ± 0.5) does not yield an increase in mobility. A more discussion on enhancement of field-effect mobility is provided in the subsequent sections, particularly during the analysis of bias dependent stress test in this manuscript. Table 1 shows extracted device parameters of all single and bi-layer devices.

Among all TFT parameters, SS value is a primary indicator of total trap density (N_t). N_t consists of bulk trap density (N_{bulk}) and interface trap density (N_{it}). The total trap density (N_t) was calculated using

following equation [22]:

$$N_t = \left[\frac{SS \log(e)}{kT/q} - 1 \right] \frac{C_{ox}}{q} \quad (2)$$

where SS is subthreshold swing, kT is thermal energy, q is the electronic charge, and C_{ox} is the dielectric capacitance of the oxide gate electrode. The calculated total trap density for (2.5 ± 0.5) nm and (4.5 ± 0.5) nm thick 1SIZO based TFT are between 1.5 to $2.5 \times 10^{12} \text{ cm}^{-2}$ whereas for device with (7 ± 0.5) nm thick 1SIZO it increases to as high as $8.9 \times 10^{12} \text{ cm}^{-2}$. Moreover, the high field effect mobility in bi-layer devices can also be ascribed to the low trap density along the drain-source current path in the conduction band region of the 1SIZO/0.5SZTO junction interface. The introduction of a high-conducting ultra-thin layer of a-1SIZO between 0.5SZTO and SiO_2 facilitates a smooth interface and establishes a highly conducting path, resulting in reduced trap density and significantly improved field effect mobility. This phenomenon can be attributed to lower effective carrier confinement at the 1SIZO/0.5SZTO interface. Further, the devices show gate leakage current in order of 10^{-9} A .

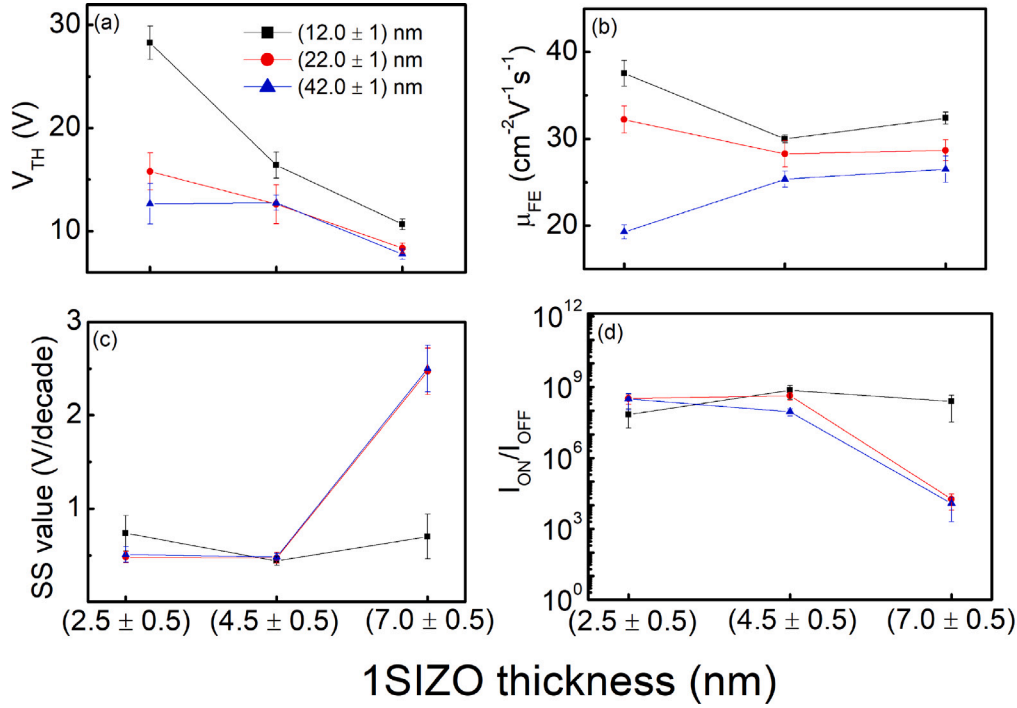


Fig. 4. Extracted device parameters of bi-layer TFTs of different thickness (a) Threshold voltage. (b) Field effect mobility. (c) SS value. (d) on/off ratio.

Table 1

Extracted device parameters of single and dual-active-layered amorphous Si-Zn-Sn-O/Si-In-Sn-O thin film transistors TFTs with different layer thicknesses.

1SIZO (nm)	0.5SZTO (nm)	μ_{FE} ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	V_{th} (V)	I_{on}/I_{off}	SS (V decade^{-1})	N_t ($\times 10^{12} \text{cm}^{-2}$)
0	23 ± 1	20.21 ± 1.5	-2.27 ± 0.50	$\approx 10^8$	0.49 ± 0.05	1.57 ± 0.03
2.5 ± 0.5	10.0 ± 0.5	37.54 ± 2.11	-28.27 ± 1.61	$\approx 10^8$	0.74 ± 0.19	2.47 ± 0.47
2.5 ± 0.5	20.0 ± 0.5	32.22 ± 3.57	-15.79 ± 1.79	$\approx 10^8$	0.48 ± 0.06	1.53 ± 0.02
2.5 ± 0.5	40.0 ± 0.5	19.27 ± 0.81	-12.65 ± 1.96	$\approx 10^8$	0.51 ± 0.08	1.64 ± 0.09
4.5 ± 0.5	7.0 ± 0.5	29.99 ± 0.46	-16.40 ± 1.28	$\approx 10^8$	0.44 ± 0.05	1.39 ± 0.04
4.5 ± 0.5	17.0 ± 0.5	28.27 ± 1.52	-12.61 ± 1.89	$\approx 10^8$	0.47 ± 0.06	1.51 ± 0.09
4.5 ± 0.5	37.0 ± 0.5	25.35 ± 0.92	-12.75 ± 0.74	$\approx 10^8$	0.48 ± 0.04	1.55 ± 0.09
7.0 ± 0.5	5.0 ± 0.5	32.37 ± 0.71	-10.66 ± 0.52	$\approx 10^8$	0.70 ± 0.24	2.34 ± 0.64
7.0 ± 0.5	15.0 ± 0.5	28.66 ± 1.50	-8.65 ± 0.50	$\approx 10^4$	2.47 ± 0.20	8.79 ± 0.50
7.0 ± 0.5	35.0 ± 0.5	26.90 ± 1.40	-8.08 ± 0.50	$\approx 10^4$	2.50 ± 0.25	8.90 ± 0.50

Fig. 5(a)–(g) show drain-source current (I_{DS}) versus drain-source voltage (V_{DS}). V_{DS} was varied from 0 to 40 V, and gate-source voltage (V_{GS}) was increased in 10 V steps from 0 to 40 V. Output characteristics show that TFT with higher field effect mobility have high I_{DS} in linear region.

To assess the temperature and electrical stability of the bi-layer TFTs, we investigated the influence of the temperature and prolonged gate bias on the drain current. The temperature was incrementally increased in 10 °C steps from room temperature to 60 °C. The transfer characteristic of the bi-layer TFTs were recorded at each temperature, with a drain bias of 5.1 V, while sweeping the gate bias from -30 V to +30 V. The source electrode was grounded during these measurements. Upon reaching 60 °C, both positive and negative gate voltage bias were applied for fixed time interval, and subsequent transfer curves were recorded. Typically, under gate bias stress, a change in V_{th} is observed due to trapping of electrons in the traps located at the bulk and interface. The trapped electrons screen the applied electric field, leading to a reduced effective applied gate voltage [23,24]. The threshold voltage of the reference single-layer 0.5SZTO-based device remains unchanged under temperature stress, while under negative bias, it exhibits a negative shift of approximately 2 V as shown in Supplementary Fig. S2.

For the temperature and bias stress tests, we randomly selected two bi-layer TFTs with different thicknesses of 1SZTO and 0.5SZTO.

Fig. 6 shows the transfer curves by temperature stress and positive and negative gate bias stress of ± 20 V. In Fig. 6(a) and (c), the device with (2.5 ± 0.5) nm thick 1SIZO has slight degradation in SS value, while the TFT with (4.5 ± 0.5) remains quite stable with an increase in temperature. A subtle degradation in SS with increasing temperature can be attributed to a formation of field-induced interface states. However, when applying positive and negative gate bias stress to the gate electrode, as depicted in Fig. 6(b) and (d), transfer curves remain almost unchanged. No variation in V_{th} for bi-layer devices under both positive and negative bias stresses suggests that the underlying ultra-thin 1SIZO layer not only establishes a highly conducting path but also mitigates the interface trap density.

4. Conclusion

In summary, we have successfully developed a high-quality low temperature RF-sputtering process for manufacturing of bi-layer oxide semiconductor TFT, comprising amorphous SZTO semiconductor with SIZO buffer layer to gate dielectric. The incorporation of an optimized ultra-thin film of 1SIZO between 0.5SZTO and the gate insulator has led to a reduction in trap density, consequently resulting in an enhancement of the field-effect mobility and stability. The thickness of both 1SIZO and 0.5SZTO layers significantly influenced TFT parameters. For bi-layer TFTs, optimal thicknesses were determined to be

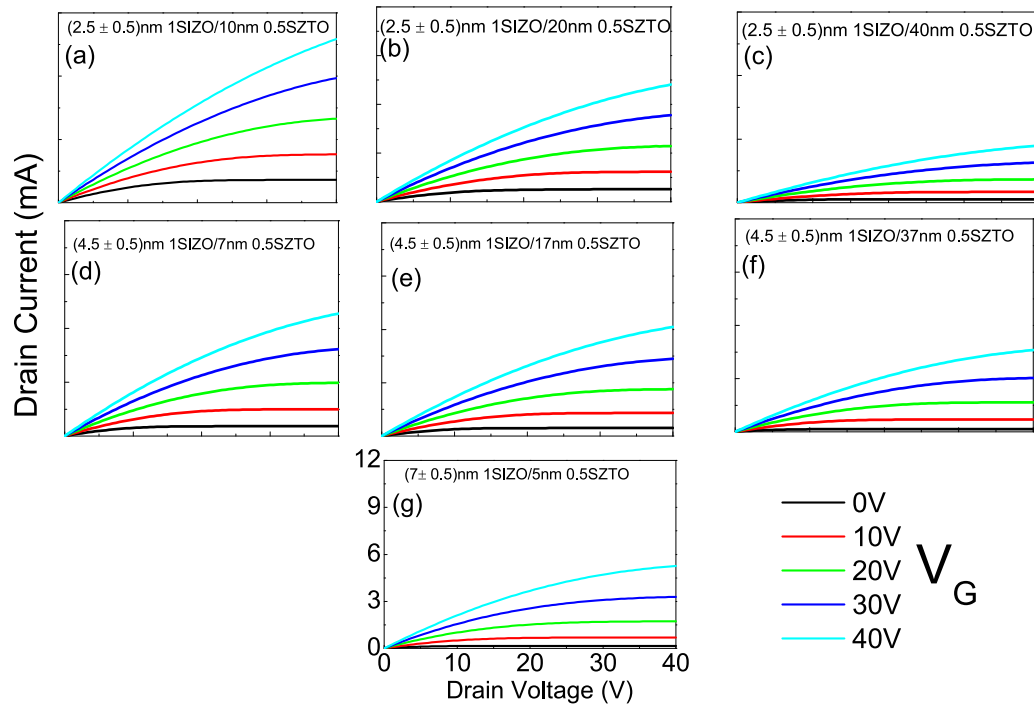


Fig. 5. Output characteristics of SIZO/SZTO bi-layer devices at different gate voltages. The scale on the y-axis (0 to 12 mA) and the x-axis (0 to 40 V) remains consistent across all plots.

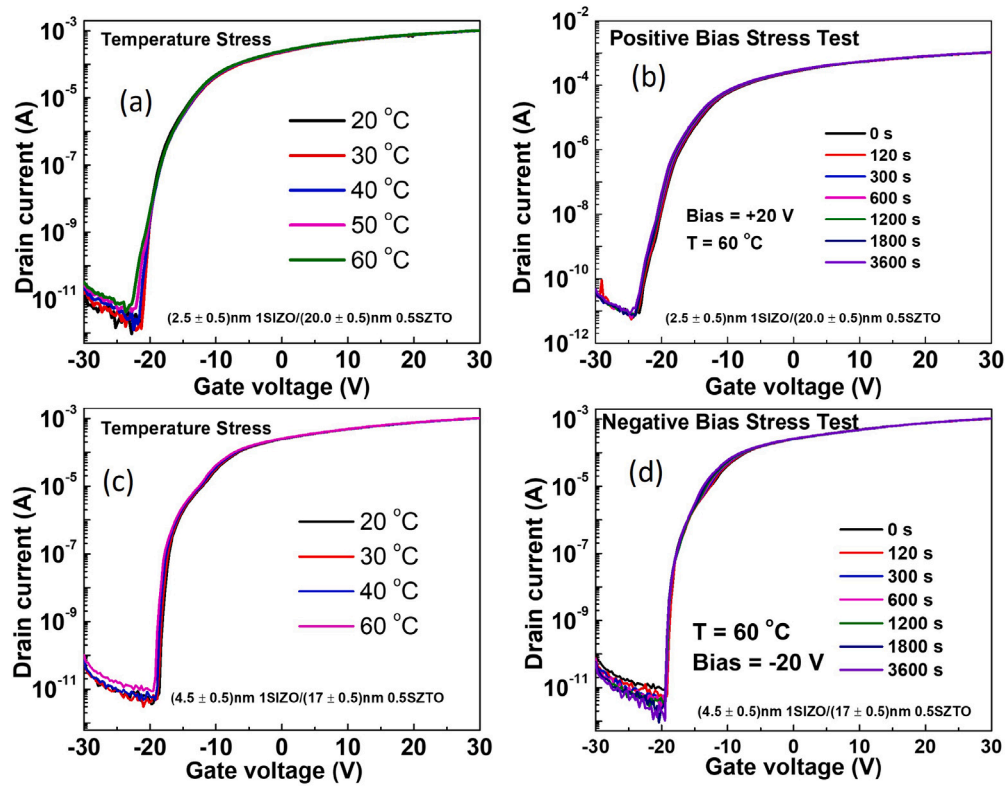


Fig. 6. Temperature stress test of $(22 \pm 1)\text{nm}$ device with SIZO thickness of (a) $(2.5 \pm 0.5)\text{nm}$, (c) $(4.5 \pm 0.5)\text{nm}$. (b) Positive bias stress test at 60 °C (d) Negative bias stress test at 60 °C.

approximately (2.5 to 4.5 ± 0.5) nm for 1SIZO and (7 to 20 ± 0.5) nm for 0.5SZTO layers. TEM images validated the thickness of the deposited bi-layer channel. The optimized bi-layer thin-film transistors (TFTs) demonstrated superior mobility ($>32 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and lower SS values compared to single-layer a-0.5SZTO TFTs. The on/off ratio for devices with a reduced thickness of 1SIZO exceeded $>10^8$. Furthermore, we investigated device stability under positive and negative bias conditions. The bi-layer TFTs exhibited exceptional stability under temperature and bias stresses of $\pm 20 \text{ V}$. This remarkable stability can also be attributed to the presence of the a-0.5SZTO layer, which also functions as an effective passivation layer.

CRedit authorship contribution statement

Sandeep Kumar Maurya: Writing – review & editing, Writing – original draft, Visualization, Validation, Resources, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Sang Yeol Lee:** Writing – review & editing, Supervision, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Sandeep Kumar Maurya reports financial support was provided by Gachon University. Sandeep Kumar Maurya reports a relationship with Gachon University that includes: employment. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Appendix A. Supplementary data

Supplementary material related to this article can be found online at <https://doi.org/10.1016/j.sse.2024.108952>.

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